# ATA Signal Path for ATA Correlator ATA-FX32 with BWRC's iBob and ADCs (by antenna by card)

Signal path designator
Zone (1-~35)
Element (a-m)
Polarization (X|Y)
Tuning (A|B|C|D)
Delay set (1-4)

Example: 13fXB3
13 refers to the "zone"
f refers to the "element" within that zone
X refers to the "polarization"
B refers to the "tuning"
3 refers to the "delay set", which defines the phasing for a beam

13f refers to a particular "antenna"
13fX refers to a particular "analog stream" on analog fiber
XB3 refers to a "beam" (or "digital stream")
13*X refers to the X-pol fibers from zone 13

ADC - BWRC's ADC Board
BET – Back End Transmitter
BPF – band pass filter
FORX – fiber optic receiver
FOTX – fiber optic transmitter
iBob – BWRC's iBob Board
LO – local oscillator
LNA – low noise amplifier
MMF – multi mode optical fiber
PABE – phased array back-end
PAM – variable gain post-amplifier module
PAX – PAM/OTX
POF – plastic optical fiber
PSP – phase switch pattern
RFCB – RF converter board
SMF – single mode optical fiber

Feed 13f
Dual linearly polarized feeds
X polarization
Y polarization
LNA
Dewar
PAM
PAX
FOTX
HPF 300 MHz
LPF 12 GHz
Analog fibers

Feed 13g
Feed 13h
Feed 13i
(…)

RFCB Chassis #1 of 4

RFCB (1 of 12)
RFCB (2 of 12)
RFCB (3 of 12)
RFCB (4 of 12)
(same as to the left)

FORX
F3dB=15.210 to 15.816 GHz
IF1 BPF
4-way splitter
Polarization X
Polarization Y
Tuning D
Tuning A
Unused
13fXD
13fXC
50 ohm coax
13fXA To Beamformer
13fYD C B A
13gXD C B A
13gYD C B A
13hXD C B A
13hYD C B A
13iXD C B A
13iYD C B A

GPS
GPS 1 PPS
GPS locked rubidium Standard
1 PPS distribution Shown below
10MHz amplified N way splitter
10 MHz
LO1A Synthesizer 16.1 – 26.7 GHz
LO1A Distribution
LO1B Synthesizer 16.1 – 26.7 GHz
LO1B Distribution
LO1C Synthesizer 16.1 – 26.7 GHz
LO1C Distribution
LO1D Synthesizer 16.1 – 26.7 GHz
LO1D Distribution
LO2 Synthesizer 14.9 GHz
L02 Distribution
LO1A:
LO1B
LO1C:
LO1D:
LO2 (for X)
LO2 (for Y)
838.8608MHz Programmable Synthesizer
6 Way Amplified Splitter
From Walsh Generator shown below
Walsh pattern Buffer drivers
PSP A
PSP B

16 Way Splitter ZC16PD-900-S
To Correlator iBob+ADC Chassis #1
To Correlator iBob+ADC Chassis #2
To Beamformer iBob+ADC Chassis #1
To Beamformer iBob+ADC Chassis #2
To Beamformer iBob+ADC Chassis #3
To Beamformer iBob+DAC Chassis #1

1 PPS From GPS
15 Way Splitter Timing Solutions 4032A
1 PPS for ADC's Sync input
To Correlator iBob+ADC Chassis #1
To Correlator iBob+ADC Chassis #2
To Beamformer iBob+ADC Chassis #1
To Beamformer iBob+ADC Chassis #2
To Beamformer iBob+ADC Chassis #3

ARM
409.6 KHz Fast Sync gen
Walsh Generator 100 Hz to 12800 Hz
To distributor in RFCB Rack (above)

Internet
48 port 10/100Mbps Layer 2 switch
To Correlator iBob+ADC Chassis #1
To Correlator iBob+ADC Chassis #2
To F chassis
To X chassis
To Beamformer iBob+ADC Chassis #1
To Beamformer iBob+ADC Chassis #2
To Beamformer iBob+ADC Chassis #3
To Beamformer iBob+DAC Chassis
To BEE2s 1..5

Ant 13f Poln X, Tuning B, W0
Ant 13f Poln Y, Tuning B, W1
Ant 13g Poln X Tuning B, W2
Ant 13g Poln Y, Tuning B, W3
Ant 13h Poln X Tuning B, W4
Ant 13h Poln Y Tuning B, W5
Ant 13i Poln X Tuning B, W6
Ant 13i Poln Y Tuning B, W7
200MHz BPF @629MHz
1PPS
Selectable Notch filter & Variable gain
838.8608 MHz Sample Clock 1

Correlator iBob Chassis #1

iBob and ADC Plate (1 of 8)
LVTTL
ADC Board (1 of 16)
ADC Board (2 of 16)
0 dBm
ADTL2-18
Sync
Clock
Atmel AT84AD001B
8 bit
reformat
16 bits @ ~400 Msps over 16 differential pairs
iBob Board (1 of 8)
Walsh Phase Un-switch
Complex Direct Digital Downconverter
Xilinx FPGA XC2VP50-7FF1517C
Data sample rate= Input ADC Sample Clock / 8
8 bits I and 8 bits Q @ ~ 100 Msps
64 bits @ ~ 100 Msps
Walsh Pattern Generator 8 square waves 100 ...12800 Hz
Ethernet
Sync Gen
Clk Gen
XAUI Core Upto 10 Gbps over Four 3.125 Gbps links

ATA-32x2 FX Correlator Sampler total is
2 iBob chassis
16 iBob plates =
16 iBob and
32 ADC Boards

iBob and ADC Plate (2 of 8)
ADC Board (3 of 16)
ADC Board (4 of 16)
Same as iBob and ADC Plate shown at the left except for Phase Switching Patterns W4, W5, W6 and W7.
Neighboring iBob and ADC plates always have completely different phase switching patterns.
iBob Board (2 of 8)

Correlator iBob and ADC Chassis #2 not shown.

Cat 6 to 48 port switch
iBob Sync, 1PPSm LVTTL
iBob Clock Sample Clock/16 = Data sample rate/2= ~ 50 MHz LVTTL
6-way Signal Translator LVDS to LVPECL
Infiniband 4x Copper cable Assembly To the I Board
Unused CX4 IEEE 802.3ak Copper cable assembly To PABE, RFI rejection,… ?
CX4 IEEE 802.3ak Copper cable assembly
Antennas 13f and 13g Polarizations X and Y Tuning B
Sync unused
Clock unused
CX4 IEEE 802.3ak Copper cable assembly
Antennas 13h and 13i Polarizations X and Y Tuning B

ATA-32x2 FX Correlator total is
1 F chassis with: 2 host computers
8 F Boards
8 C Boards
1 I Board
1 X Chassis with 2 host computers
8 X Boards
8 C' Boards
And 32 CT cables

FX 32 rack

F Chassis
Cu_Rx (2 of 2)
Cu_Rx (1 of 2
F Board (8 of 8)
F Board (1 of 8)
Xilinx FPGA XC2VP40-6FF1152C
8 complex 1024 point 6-time overlap PFBs
4-way Corner Turner
ZBT SRAM
F7 F6 F5 F4 F3 F2
Linux Host Computer 2 of 2
Linux Host Computer 1 of 2
Compact PCI bus 2 of 2
Compact PCI bus 1 of 2
C Board (8 of 8)
C Board (1 of 8)
20x2 conn
Xilinx FPGA XC3S2000-4FG900C 8 way corner turner
256 pin edge conn
C 7 C 6 C 5 C 4 C 3 C 2
I Board
Corner Turner slot to slot interconnection buses and 12 way low skew drivers for 6 "clocks"

X Chassis
X Board (8 of 8)
X Board (1 of 8)
Xilinx FPGA XC3S5000-4FG900C X Engine
ZBT SRAM
X7 X6 X5 X4 X3 X2
C' (8 of 8)
C' (1 of 8)
Passive Hardwired interconnect
C' 7 C' 6 C' 5 C' 4 C' 3 C' 2

Cat 6 to 48 port switch
Cat 6 Network cable

Each X Board gets a 1/8th the spectral channels from all the antennas. The data path of the example antenna, 13fXB, is no longer highlighted in yellow.

Corner Turner cable assembly Bundle 8 of 8
Corner Turner cable assembly Bundle 1 of 8
Clock, sync and 16 data bits 18 LVDS pairs over each twisted pair Cable assembly at ~ 100 MSPS

Infiniband 4x Copper cable Assembly From the 6 way Signal Translator

DRD – 5/20/2005
MRD – 2006dec08
MRD – 2007jul16
MRD – 2008jan24
MRD – 2008sep18