

Extended core storage for the control data 64 6600 systems

by GALE A. JALLEN
Control Data Corporation
Minneapolis, Minnesota

INTRODUCTION

The software operating systems for the Control Data 64/6600 Extended Core Storage (ECS) have been described in another paper.¹ The ECS is organized basically as a very large word two wire magnetic core memory with multi-phased banks. The use of multi-bank phasing and very large memory word construction has allowed the basic core to operate at a reasonable, cycle time of 3.2 microseconds while providing an average data rate of 600 mega bits per second. The purpose of this paper is to describe the design of the basic memory hardware required to operate a very large word memory.

Hardware system description

The memory system is organized in logically independent banks of 125 K words. These banks are made up of 16,384 memory words of 488 bits each. The 488 bit word consists of eight 60 bit computer words plus 1 bit of parity for each computer word. It is a conventional two wire word organized magnetic core system with a cycle time of 3.2 microseconds for each of its 488 bit memory words. The access time to this word is approximately 1.6 microseconds measured at the controller interface. This bank represents the smallest available size for ECS and also the slowest data rate of 150 mega bits per second. Four of these banks can be phased to provide a capacity of 500 K words of 60 bits each and a maximum data rate of 600 mega bits per second. The four banks are housed in one cabinet similar to that of a 6600. Four of these cabinets or bays can then be interfaced with the central processor by means of the controller channels to provide up to 2×10^6 words of core memory.

Figure 1 shows the basic data flow diagram for 1 bank of ECS. Beginning with the CPU coupler in the central processor, the responsibilities assigned to it are: to generate and assemble the ECS address and

word count, to update the ECS address for each eight word record transfer, and to provide any necessary ECS and central memory data transfer housekeeping. The ECS coupler communicates with the controller on a 60 bit bidirectional data bus and an independent 24 bit address bus. The controller contains several function responsibilities. It contains a sequential scanning mechanism to service four 60 bit bidirectional data channels from CPU couplers and also four 60 bit bidirectional channels to ECS core store I/O registers. The requests are honored in sequence at the end of each eight word record transferred. Only one data path through the coupler is provided. This data path contains a parity generator with which parity is generated and checked as data is passed through the controller. The status of this parity is transmitted back to the CPU coupler. Since the ECS

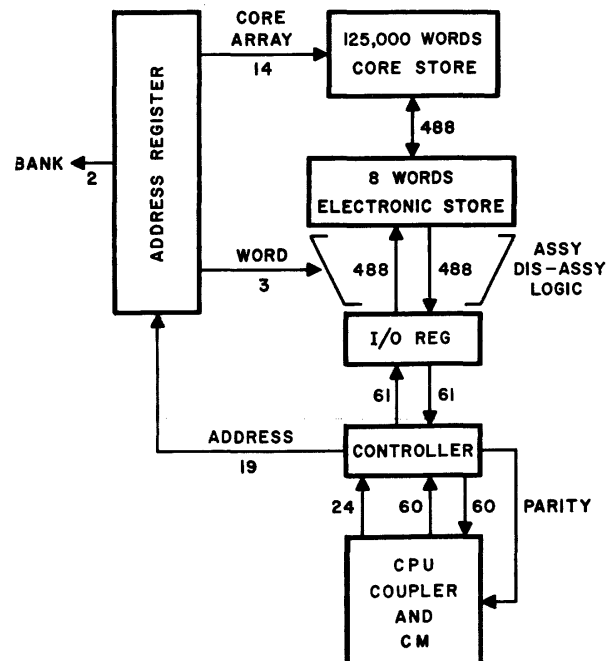


Figure 1

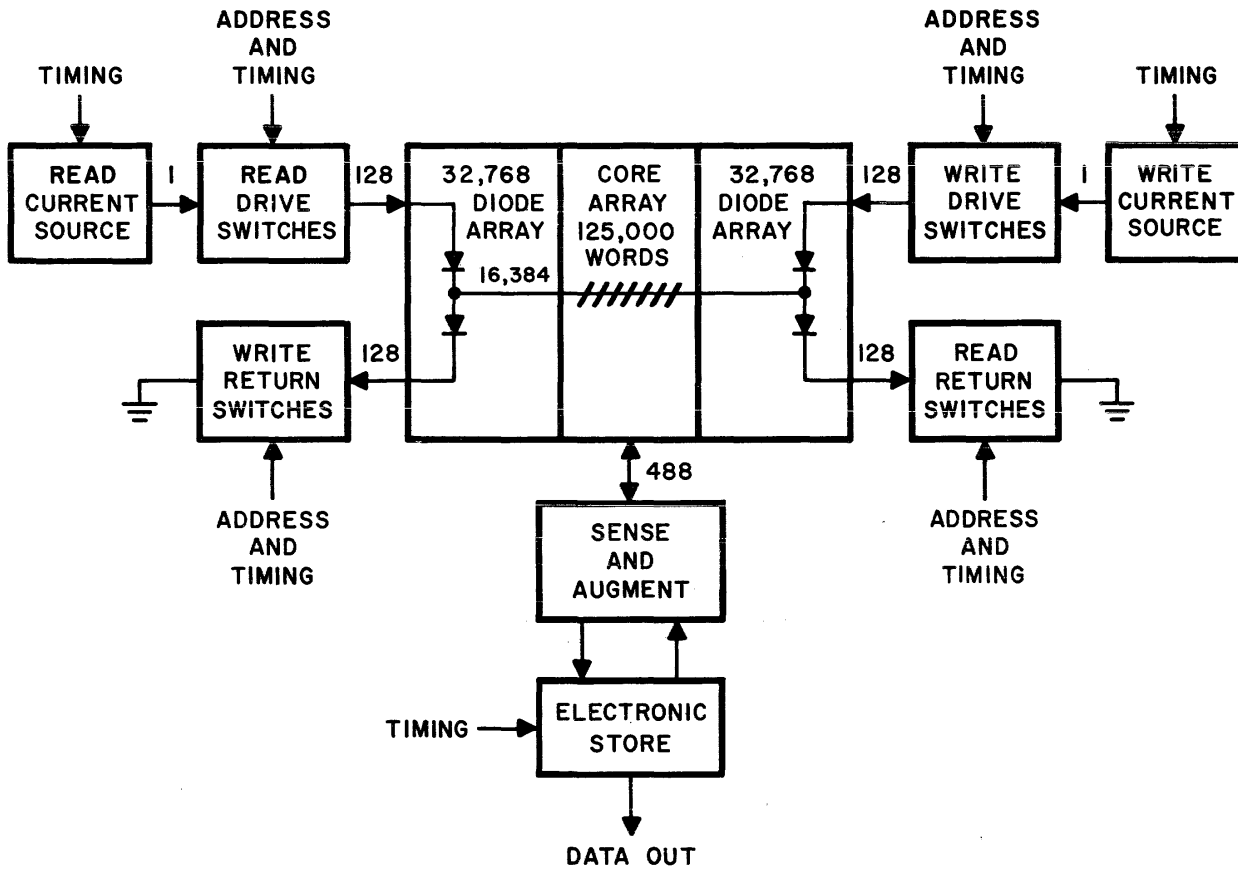


Figure 2

is a synchronized memory system, the controller contains the system master clock which controls all ECS bays and all CPU devices connected into the system. A portion of the 24 bit address information which is sent from the CPU coupler is decoded at the controller to select the bay address. A bay of ECS is 500 K words. The controller also contains ECS core housekeeping logic which provides the necessary timing to insure that no shorter period than 3.2 microseconds occurs between requests to any ECS bank. Moving up through the signal flow on Figure 1, we now communicate with the ECS I/O register. This 60 bit I/O register is shared by the four ECS banks in each bay. The I/O register communicates with the eight words of electronic store through assembly and disassembly logic. This logic is addressed by 3 bits of the ECS address and allows the selection of any part or all of the eight words of the electronic store. The eight words of the electronic store are duplicated for each bank of core memory. The electronic store provides a buffer for holding the data while another bank is being cycled 800 nano-seconds later in a multi-bank phased system. The electronic store also provides the necessary buffer for the recirculation of the data back into store. If

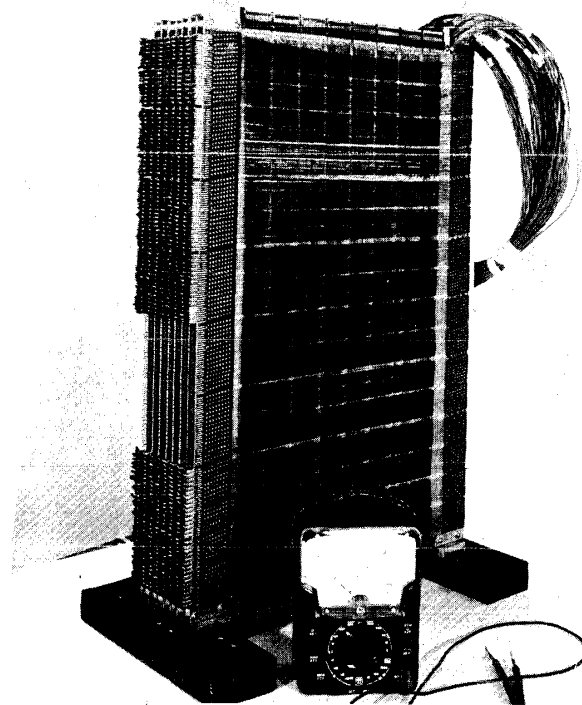


Figure 3

less than eight words are addressed in a write mode, this register recirculates the remaining words back to core on either a read or write operation. The eight words of the electronic store communicate through the sense amplifier augment generator system of the core store which in turn communicate directly with the magnetic core elements. It is this portion of the memory which I will describe in more detail.

Hardware description

Referring to Figure 2 shows the basic block diagram of the ECS core memory proper. The heart of this block diagram is of course the central core array consisting of approximately 8×10^6 cores and their associated selection diode arrays. These items are combined in one core stack system. A picture of this core stack can be seen by referring to Figure 3 which includes a standard voltmeter for size comparison. It is basically 30 inches by 20 inches by 6 inches in size. The basic storage element used is a 30 mil core with a total switching period of approximately 500 nanoseconds. These cores are then mounted on both surfaces of a plane of approximately $\frac{1}{2}$ million cores per side. Also integral with this plane are the word selection diodes.

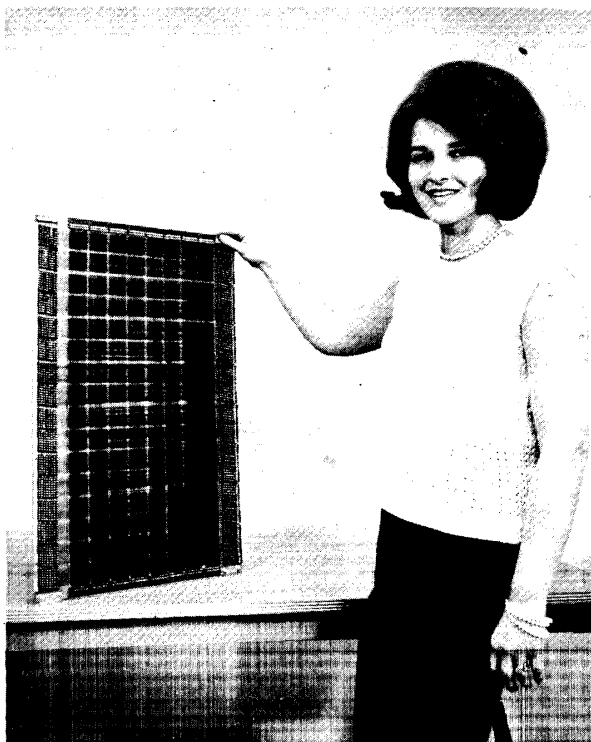


Figure 4

Figure 4 shows a picture of a core plane. Visible in the photo are approximately 5×10^5 cores. They are mounted on a copper ground plane. Along the long dimensions are the selection diodes which form the

terminations for the word wires. Along one long dimension edge and both short dimensions are the interconnecting connectors. These connectors are used during plane testing as well as semipermanent stack assembly connections. The back side of the plane consists of an identical set of cores and diodes resulting in a plane assembly of 1×10^6 cores. These plane assemblies are complete units which can be tested and repaired independently before being assembled into stacks. The word selection diodes were placed on the plane assemblies in order to reduce the total number of interconnecting wires required to assemble these planes into a stack of approximately 8×10^6 cores. These diodes are the only electronic assemblies mounted in this area. Approximately 100 watts of power is dissipated in this stack during a write operation. This heat is removed by a low velocity air stream pulled through the stack by small fans located on the edge of the stack which draw cool air from the chilled logic card area which is Freon cooled in the 6000 systems. The assembly of eight planes of 1×10^6 cores each into a stack results in a total bidirectional word drive matrix of 128 by 128. No attempt was made to break this large diode matrix down into smaller portions. Electronic means were used to reduce the effects of the very large capacitance resulting in this array.

Referring to Figure 5, a simplified schematic of the word drive matrix is shown with some of the stray capacitances placed at their physical locations. The primary path for current flow during the read portion of the cycle is shown in bold. A generator labeled back emf is shown in series with the selected line and represents the total output of all cores being switched from "1" to "0" state. Since each core produces approximately 50 millivolts, the maximum back emf reaches 25 volts when all 488 bits are in the "1" state. Added to this voltage are diode and IR drops which bring the total to 30 volts. Conversely when all bits are in a "0" state, the total drop reduces to approximately 7.5 volts. This variation in load on the constant current source requires that it have a high output impedance in order that the "bite" into the read current will not be large enough to increase the switching time of the cores as "1's" are added to the word. The typical "bite" experiences on ECS is in the order of 5% when the core switching time totals 350 nanoseconds. This represents a total drive system shunt impedance of approximately 1 K ohm at the core switching frequency of approximately 2.0 megacycles. Referring again to Figure 5, it can be shown that a parasitic capacitance of some 3800 pico farads exists in the drive matrix which is potentially in shunt with the read current source. At 2.0 megacycles this would

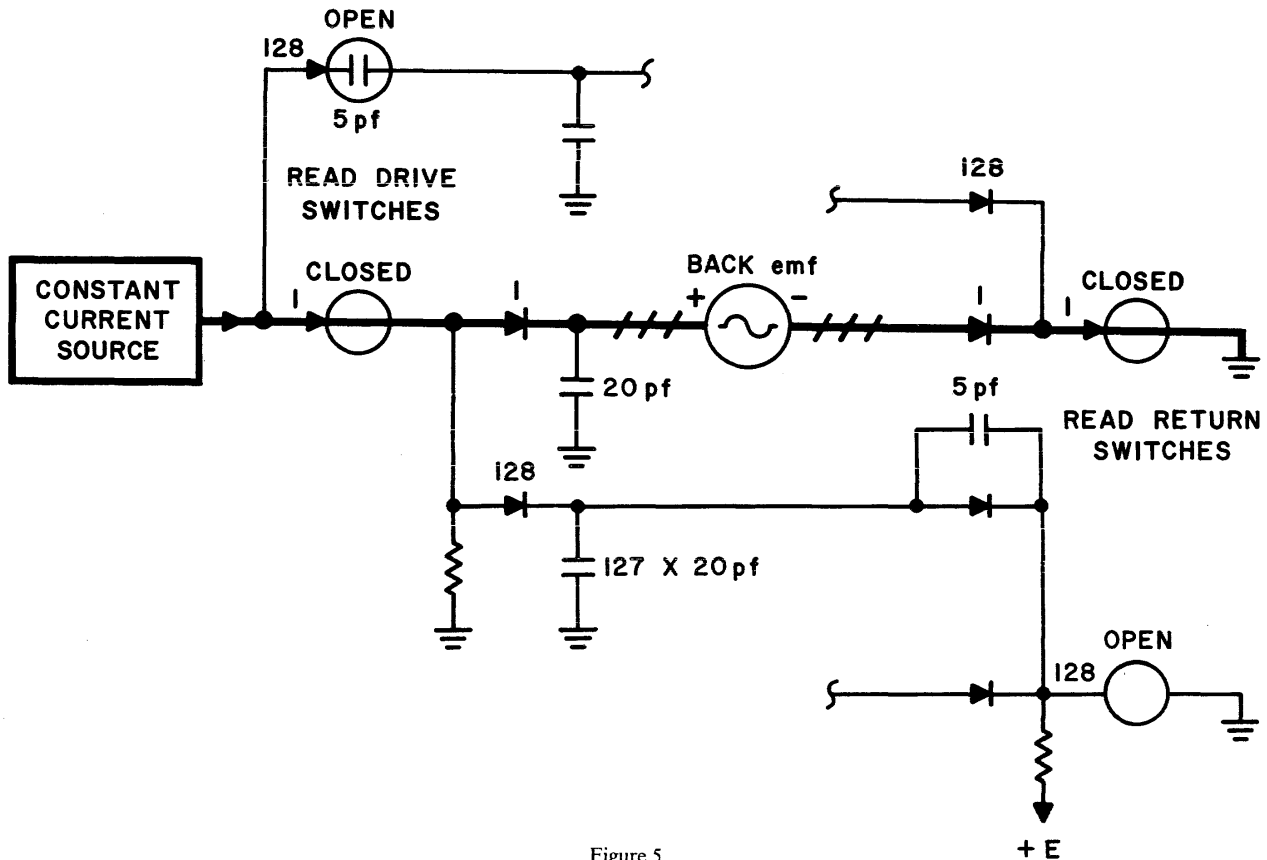


Figure 5

be approximately 21 ohms of shunt reactance, an impossible situation. A system of preconditioning is used in the drive system to reduce by approximately fifty to one the effect of this shunt capacitance. Since some form of damping is required on any LC network,

and the condition for critical damping is $R = \frac{1}{2} \sqrt{\frac{L}{C}}$

it becomes apparent that reduction of the effective capacitance allows a higher damping resistance to be used to further increase the effective shunt impedance in the drive system.

Only one read current source is used by the entire ECS bank. The timing and rise time characteristics of this one source determine the entire core array timing. This current source is steered through transformer coupled drive switches. Since these switches are A.C. coupled, any failure of the timing mechanism cannot sustain current in the core array and cause serious damage. As can be seen by referring to Figure 2, two sets of switches are required to provide a path for the current through this core array. All the switches used can be divided into two categories, the read drive switches and the return switches. They are identical in characteristics except for the common terminal, in one case the positive collector is common and in the other case the negative emitter is common

in the switch. The write current drive is identical to the read current drive except for timing and magnitude. In general, the word drive system can be considered quite conventional in the state-of-the-art except for the burden of the large array capacitance and large back emf resulting from long core words.

Referencing Figure 6 shows a simplified schematic of the sense digit system showing the folded sense line. This line totals approximately 40 feet of wire and has 16,384 cores on it. One-half of the 16,384 cores are on each half of this line and are sensed at the end by means of a differential sense amplifier which has A.C. coupling to provide low frequency roll off. Since the sense line is approximately 40 feet long, a rather long propagation delay results and a somewhat peculiar problem of core output summing in the differential amplifier occurs. Cores located at one end of the digit line would appear reduced in output since the positive or negative input to the differential amplifier would be displaced in time before being added in the amplifier. This reduction in output would not occur on cores located near the center of the digit line since both inputs would be delayed an equal amount. This variation in output can be controlled by specifying a core switching time that is long with respect to the digit line propagation delay.

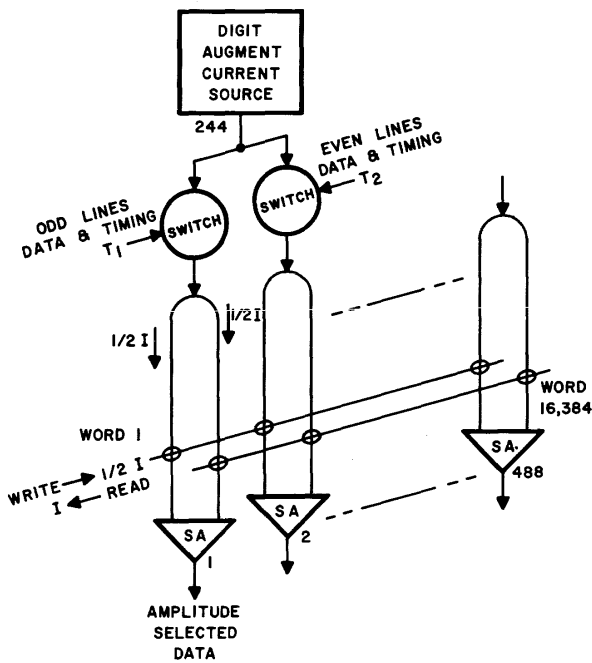


Figure 6

The variation experienced on ECS with a 200 nanosecond propagation delay and a core switching time of 500 nanoseconds is less than 30%.

In order to reduce the length of all lines involved in the core stack, the 30 mil cores were placed on 25 mil centers in both coordinates. This close spacing results in a large mutual capacitance and inductance between adjacent digit wires.³ A large signal crosstalk and a data dependent digit line characteristic impedance are two deleterious effects of these high mutuals. To reduce the effect of these mutuals, the core mats were placed on a substantial ground system and a sequential odd-even digit line drive was incorporated. Sequencing the digit line drive reduced the mutual capacitances and inductance by doubling the effective digit line spacing. As can be seen in Figure 6, this sequencing also allowed the sharing of digit current sources. This sharing reduces the digit D.C. power 50% by reducing the peak digit current required. The simultaneous drive of 244 digit line pairs results in approximately 120 amperes of current flow through the digit lines and stack ground system during a write operation. In order that recovery from this large transient be effected quickly, all effort was made to maintain a stable characteristic impedance in the digit system of ECS. The results of this effort produced a recovery time of less than 1 microsecond.

Mechanical construction

Referring to Figure 7, a picture of the ECS chassis can be seen. For those familiar with the 6000 series computer construction,⁴ the ECS chassis is identical

in that a Freon cooling system is used and all logic is constructed on cordwood packages using silicon logic. Approximately 3 ton of refrigeration capacity is required to cool four ECS banks. The waste heat from these systems is carried away by chilled water. Except for the 60 cycle Freon compressor, all power for ECS operation is obtained from a 400 cycle power system. The logic power supply is mounted integral with each chassis. The digit drive power is located remote in the cable exchange area at the end of the ECS cabinet. Four of these power supplies are located in this area, one for each ECS bank.

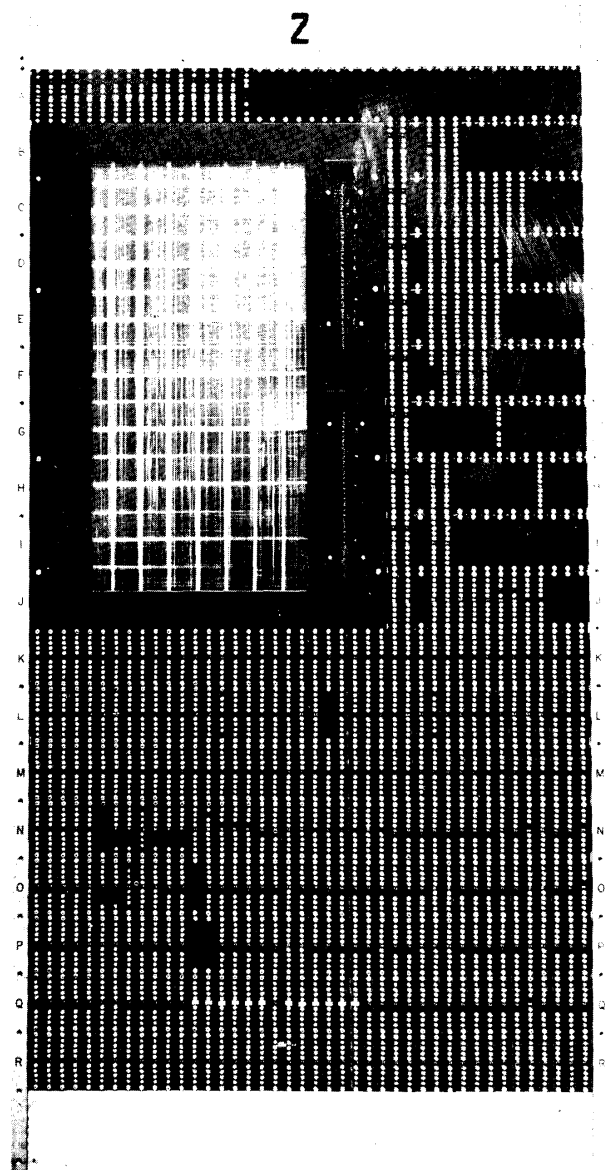


Figure 7

Maintenance

Several maintenance features are included in ECS. All power supplies are made adjustable at the maintenance panel. The purpose of this feature is to help detect potentially marginal situations during scheduled maintenance periods.

A procedure for "graceful degradation" is available. The purpose of this feature is to keep the addressing continuous by pushing down higher order addresses to replace terminated lower order addresses. The effect upon the user is to maintain a continuous address field by accumulating all terminated addresses at the higher order end of the address field. Implementation of this feature requires a minimum of down time and allows the accumulation of several failures before major repair is scheduled.

CONCLUSION

Block transfer or streaming data flow has effected a new approach to memory design. The 64/6600 ECS

has taken advantage of this streaming data flow to improve the efficiency of the memory by providing very high capacity and data rates at low cost per bit. Although the ECS was optimized for block transfers, good performance in a random mode is also possible.

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