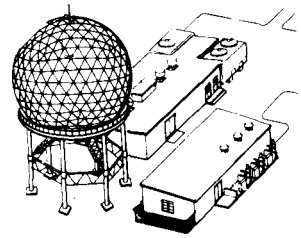


LESSON 3. HIPAR ACQUISITION RADAR

MMS Subcourse No 150 . . . . . **Nike Radars and Computer**

Lesson Objective . . . . . **To give you a general knowledge of the purpose and basic functions of the AJI HIPAR on a block diagram level.**

Credit Hours . . . . . **Four**

TEXT

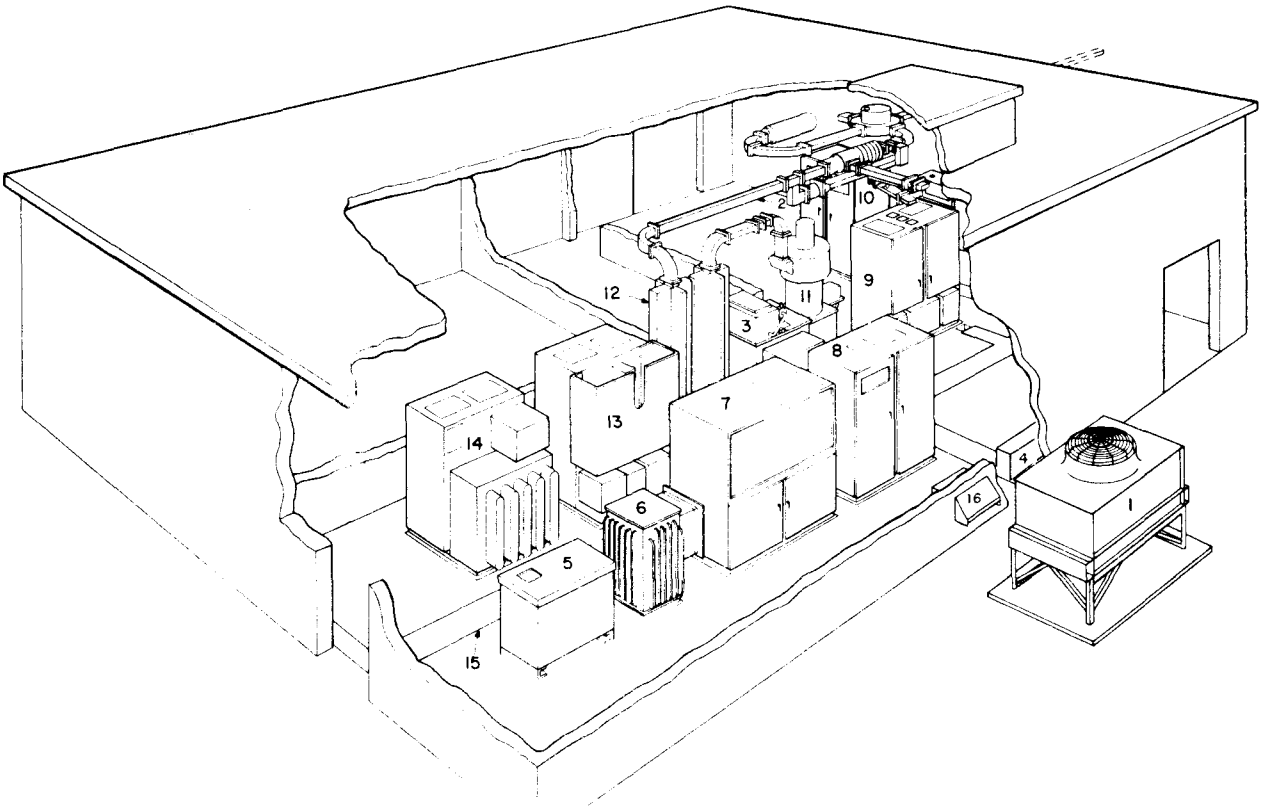
1. PURPOSE.

a. The AJI Hipar system, a major component of the improved Nike-Hercules system, is a complete microwave range and direction sensing system. The primary function of the HIPAR system is to locate, interrogate, and designate, to the target track radar (TTR), targets in the area defended by the improved Hercules system. The HIPAR system can detect air to surface missile (ASM) or tactical ballistic missile (TBM) type targets.

b. The HIPAR system supplies acquisition target video and certain mark signals to the TTR. The signals represent target slant range and azimuth information. When a designated target is within range of the TTR, the coarse slant range and azimuth of the target can be transferred to the TTR. Since the range of the HIPAR is greater than the range of the LOPAR, more time is allowed for evaluating the target, for designating it to TTR, and for making a greater number of intercepts if HIPAR is the selected acquisition radar. Additional information is available through the use of SIF/IFF equipment associated with each acquisition radar and FUIF equipment which was discussed in the LOPAR lesson.

c. When both HIPAR and LOPAR are used, they share the presentation system discussed in the LOPAR lesson. The presentation system is capable of displaying video and target position data from either radar through operation of the acquisition radar-select circuits. In addition, the presentation system furnishes designated target position data from either the HIPAR or LOPAR to the TTR system. Selection of the acquisition radar depends on the tactical situation. When both radars are brought to operational status, negligible time is lost in switching from one to the other. The sharing of a common presentation system by both acquisition radars necessitates the switching of preknock, sync, antenna position, IFF, and acquisition video signals to coordinate the display of targets. Synchronization of the TTR with the selected radar is accomplished by switching the preknock pulses to the acquisition-track synchronizer in the TTR. Thus, targets can be acquired by TTR regardless of which acquisition radar is operational.

d. The HIPAR building (fig 1) contains all the equipment for the HIPAR system, except the HIPAR antennas and the antenna radome-support tripod. System serial numbers 538 thru 594 are represented by figure 1. The numbers in parentheses (fig 1) are the



1. Liquid cooler (47)
2. Antenna coupler (74)
3. Pumping unit (53)
4. HIPAR Interconnecting box
5. Step-up power transformer (86)
6. Induction voltage regulator (80)
7. Power control-indicator (75)
8. Control-oscillator group (63)
9. Receiver group (73)
10. MTI group (22)
11. Klystron amplifier (76)
12. RF harmonic filter (85)
13. High voltage pulse generator (78)
14. High voltage power supply (79)
15. Electrical cable assembly set (81)
16. Simulator distribution box (87)

Figure 1. HIPAR building and equipment.

major unit numbers of the HIPAR system. In addition to the fixed installations, represented by figure 1, the HIPAR has been produced in a mobile configuration (serial numbers 801 and above). The mobile system contains the same major units as systems 538-594. Three vans, two trailers and their prime movers are required for the mobile system.

2. SYNCHRONIZER SYSTEM.

a. **General.** When the HIPAR is selected to provide acquisition data for the improved Nike Hercules system, the synchronizing system produces timing pulses that synchronize operations throughout the RCDC. These timing pulses initiate radar-transmit RF burst, provide range determination references, synchronize presentation system display, and maintain a uniform time reference for system operation.

b. **MTI trigger generation.** In the AJD (normal) mode of operation the MTI system produces the master timing pulses of the synchronizing system. MTI trigger generation circuits (B9, fig 2) may produce stagger triggers or non-staggered triggers. When the HIPAR is operated in the basic receiver (standby) mode the MTI trigger generation circuits are not used and the synchronizing system is permitted to free run. When the HIPAR is operated in the pulse-to-pulse mode the

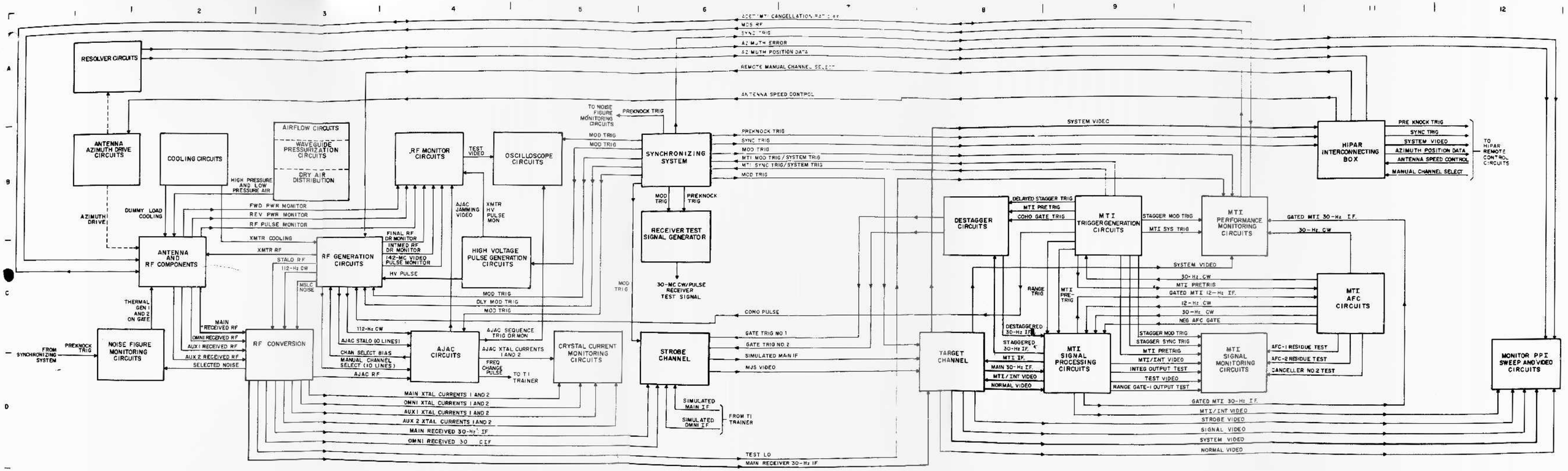
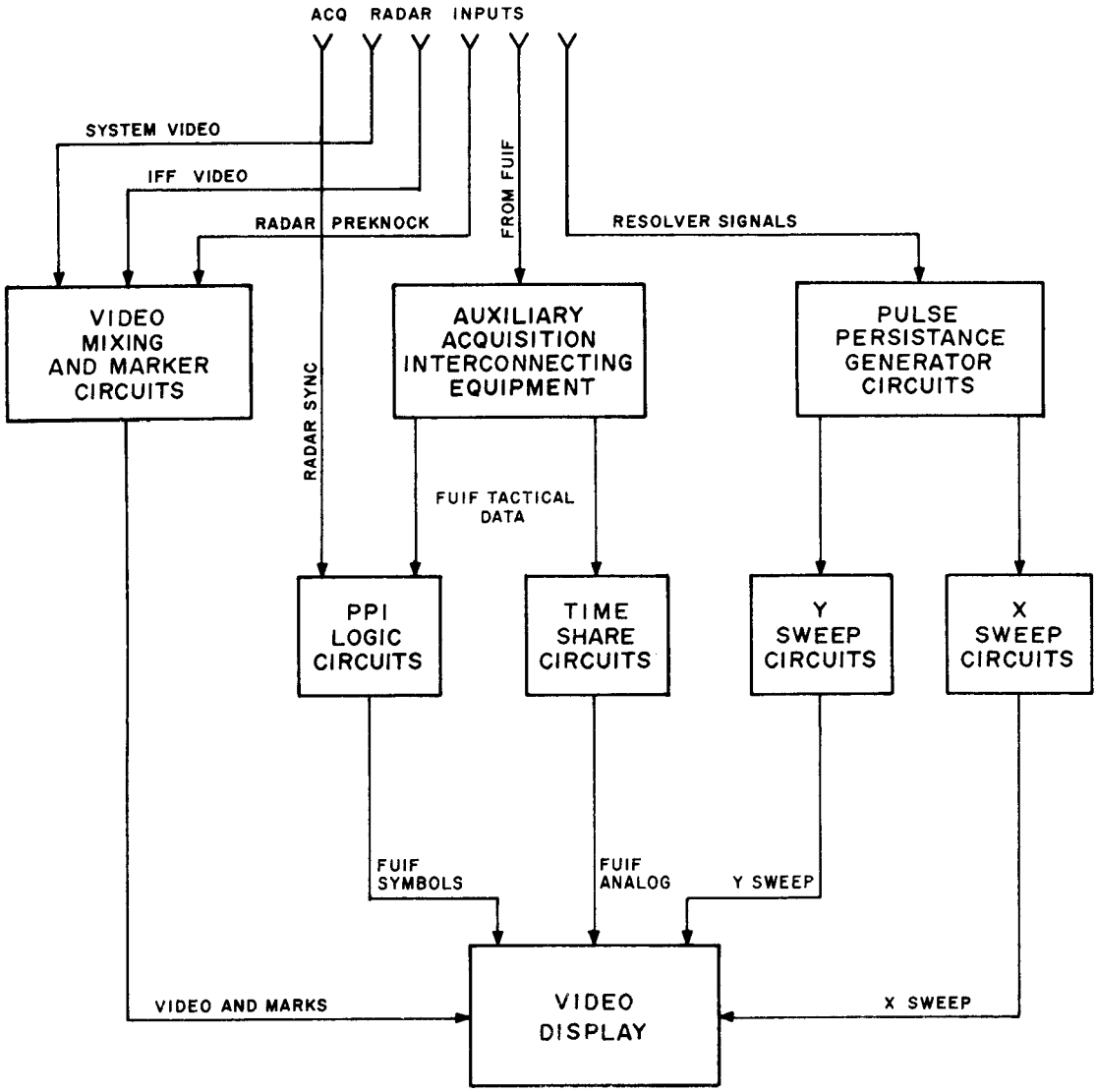


Figure 2. AJ/JATBM HIPAR system block diagram.



BCC PRESENTATION SYSTEM

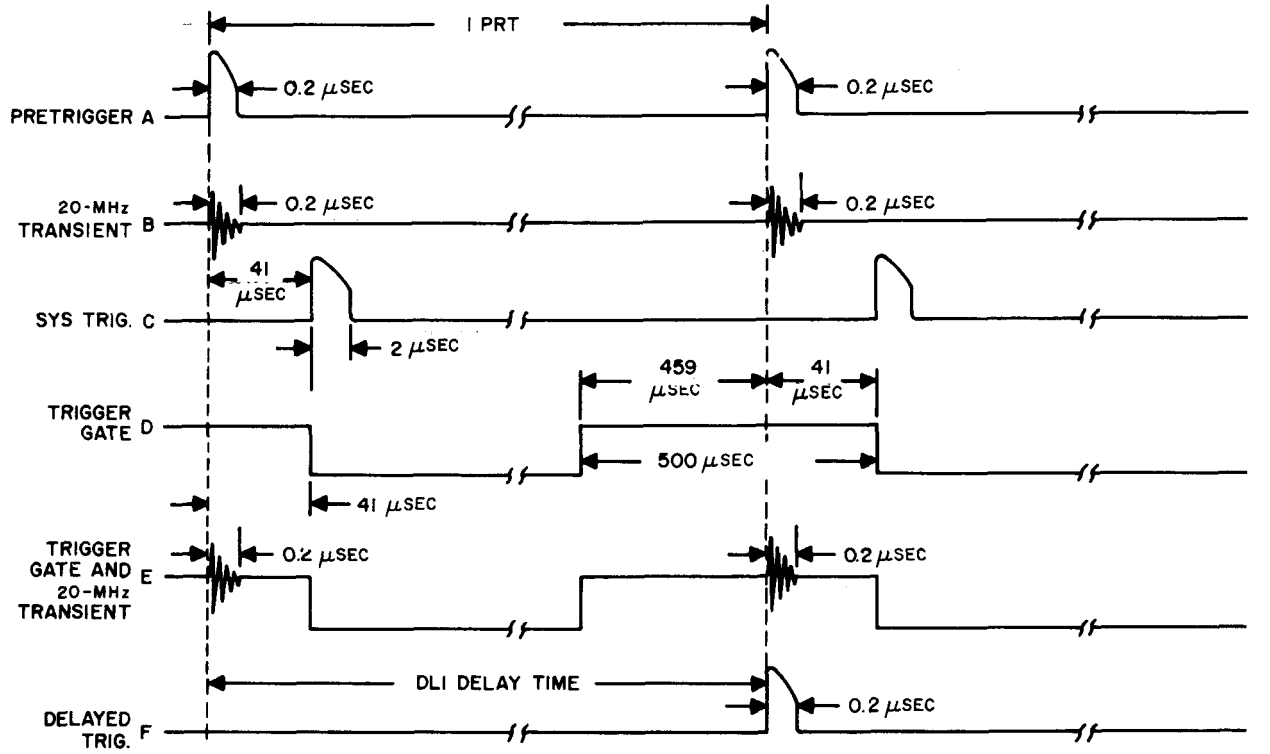


Figure 3. MTI pretrigger and MTI system trigger circuits - timing diagram.

synchronizing system is timed at a random rate. During normal operation, MTI pretrigger (A, fig 3) is the basic timing pulse. The initial MTI pretrigger is developed from a blocking oscillator. This blocking oscillator pulse shocks an RF amplifier into oscillation to generate a 20 MHz transient pulse (B, fig 3). The blocking oscillator output is also applied to a 41-microsecond delay line to produce MTI system trigger (C, fig 3). The MTI system trigger is applied to a monostable multivibrator to initiate a guard gate (D, fig 3). The 20 MHz transient pulse is applied thru a 1-PRT delay line to an RF amplifier. The 20 MHz transient is gated through the RF amplifier during the positive excursions of the guard gate, resulting in a gated transient (E, fig 3). The 20 MHz transient is detected, resulting in a delayed trigger (F, fig 3), which is applied to the blocking oscillator to complete the delay loop and synchronize MTI pretrigger with a PRT equal to the time of the delay line. The guard gate allows time sharing of the delay line with circuits in the MTI system. Both MTI pretrigger and MTI system trigger are applied to stagger circuits within the MTI trigger generation circuits. After processing in the stagger circuits the unstaggered MTI system trigger is applied to the trigger synchronizer in the synchronizing system if stagger is off (B6, fig 2). During normal operation with stagger on, the trigger selection circuits apply stagger sync trigger and stagger mod trigger to the trigger synchronizer.

c. **Trigger selection circuits.** The trigger selection circuits in the synchronizer system (B6, fig 2) consist of relays and switches that are used to determine the HIPAR mode of operation. Mode relays are controlled from the HIPAR building when the radar is in the test condition and from the trailer mounted director station during the operate condition.

(1) Basic receiver or standby mode. During the basic or standby mode of operation all inputs to the trigger synchronizer circuits are removed by the select relays. In this mode the trigger synchronizer is a free running system and produces the timing pulses for the HIPAR. The MTI is turned off.

(2) AJAC pulse-to-pulse mode. In the AJAC pulse-to-pulse mode the trigger synchronizer is activated by the application of a random trigger from a jitter generator. The jitter generator is located in the synchronizing system (B6, fig 2) and establishes the PRT of the HIPAR at a random rate. The MTI is turned off in this mode also.

(3) Normal mode (stagger on). During stagger on (alternately long and short PRT operation) MTI system trigger (B9, fig 2) is staggered by the stagger circuits to develop stagger sync and stagger mod trigger which are applied to the trigger selection circuits. During

stagger PRT operation, the trigger sync circuits are synchronized by stagger sync and stagger mod trigger.

(4) Normal mode (stagger off). During stagger off (steady PRT operation), the MTI system trigger is the basic timing pulse for the HIPAR. All outputs from the synchronizing circuits are synchronized by the MTI system trigger. The time relationship of these outputs may be seen in figure 4.

(5) Coherence (COHO) pulse generation. When the HIPAR is in the normal mode of operation a 30 MHz COHO signal generated in the MTI is gated to the transmitter by the MTI trigger generation circuits (B9, fig 2). The COHO pulse is used to phase lock the transmitter for proper phase relationship to perform cancellation of stationary targets.

d. Stagger circuits.

(1) The stagger circuits, which are part of the MTI trigger generation circuits (B9, fig 2), are used to vary the time interval between transmitted pulses. Staggering of the time interval prevents loss of certain targets due to MTI cancellation at radar blind speeds. Radar blind speed is a problem peculiar to any MTI system using the coherent cancellation of the target return. Coherent cancellation is a function of the difference in phase of target returns on successive PRTs. In the MTI system the main received IF signal is delayed one PRT and shifted 180 degrees in phase, then added algebraically to the next PRT IF return. If the reflection is from a stationary object, the delay and nondelay IF signals will possess a constant out of phase, equal amplitude relationship and cancellation will occur. If the reflection is from a moving target, the phase characteristics of each return RF is different from pulse to pulse, resulting in incomplete cancellation. The residual signal is developed into MTI video which represents a moving target. However, if a target is moving the distance of one-half wavelength during one PRT, the reflected signal will exhibit the same characteristics as if the target were stationary. Thus, a radar using phase cancellation MTI would not produce a video pulse for a target moving at the radar blind speed. In looking at the formula V_b= PRT it can be seen that the blind speed V_b is a function of transmitter frequency and pulse repetition time. It can also be seen that if the PRT is changed the blind speed will be changed. By staggering the PRT, from a base time, the threat from blind speed can be removed.

(2) The MTI pretrigger, MTI system trigger and the 30 MHz CW from the MTI system are applied to the stagger circuits. The stagger circuits, within the MTI trigger generation circuits, contain the following circuits: ringing pulse generator, multiplexer, 35.3 microsecond delay line, electronic switch and two trigger pulse amplifiers. From MTI system trigger, the stagger circuits generate alternately long and short PRTs by applying a 35.3 microsecond delay to develop stagger mod trigger and ringing and COHO pulse (fig 5) during one cycle and removing this delay during the next cycle. Stagger sync trigger (occuring at a steady PRT) is always delayed 35.3 microseconds from MTI system trigger. During the normal mode with stagger on, ringing and COHO pulse and stagger mod trigger develop a staggered COHO pulse and a staggered mod trigger output from the synchronizing system. Delay mod trigger is also staggered. The other outputs (fig 6) from the synchronizing system are developed from stagger sync trigger. These signals, preknock trigger and sync trigger, are generated at a steady PRF with stagger on (B6, fig 2).

3. TRANSMITTER SYSTEM.

a. Purpose. The transmitter system produces high power RF pulses that are radiated into space by CSC^2 or FAN acquisition antenna. Selection of antennas depends on the tactical deployment required. Circuits internal to the transmitter are used to determine the transmitter pulse width and the frequency contained in this pulse. The mod trigger, delay mod trigger, and COHO pulse determine whether the transmitter RF is produced at a staggered or steady PRF (stagger on or off).

b. RF generation circuits.

(1) The 30-MHz COHO pulse (C3, fig 2) is amplified and mixed with a 112-megahertz CW to form a 142-megahertz pulse. The 142-megahertz pulse is gated into an RF mixer by a gate voltage initiated by mod trigger. The gated 142-MHz pulse is mixed with a STALO RF (stable local oscillator) to produce an intermediate RF drive in the L band frequency range. The intermediate drive is amplified by a traveling wave tube and applied to a pulse amplifier modulator. The pulse amplifier modulator, synchronized by the delay mod trigger, reduces the duration and amplifies the intermediate drive to produce final RF drive. The delay of the delay mod trigger (F, fig 5) is adjustable from 0.3 to 6 microseconds for centering final RF drive under the high voltage pulse from the high voltage pulse generation circuits. During basic receiver or standby operation, the COHO pulse is removed from the RF drive circuits and an internally generated 30-MHz signal is used in the formation of final RF drive.

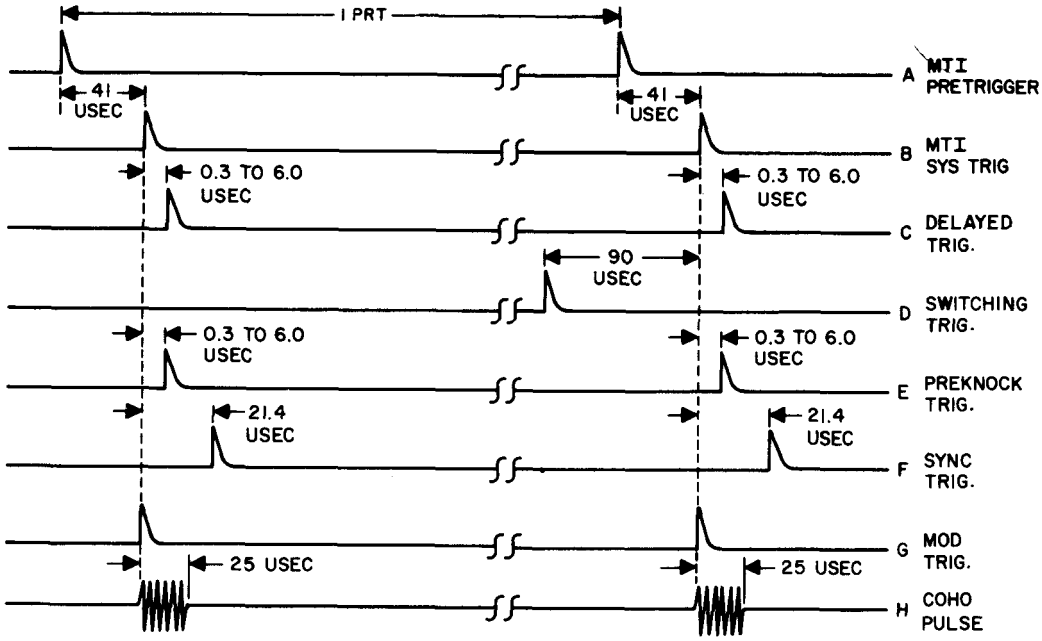


Figure 4. Synchronizing system - stagger off operation - timing diagram.

(2) Rapid changes in the frequency of final drive are permitted through the use of a STALO electronic switch and a number of crystal oscillators and frequency multipliers. The oscillator and multiplier circuits produce the STALO RF signal. Frequency change action may be initiated manually by depressing a frequency change switch or automatically through the AJAC circuits (C4, fig 2). Actual changing of frequency is delayed until radar dead time. The delay for changing frequencies is accomplished in the AJAC circuits. Cutoff bias (channel select) on the selected STALO is removed, thru the action of the frequency change circuits, permitting an output frequency to be amplified and multiplied. Bias is removed from only one STALO at any instant; therefore only one final RF drive frequency is available during any period of time. Manual changing of frequencies may be made from the power control indicator (major unit 75) with the radar in test condition or from the trailer mounted director station-battery control console with the radar in the operate condition. AJAC selection of frequencies can only be made with the radar in the operate condition. The STALO RF and 112-MHz CW signals produced in the RF generation circuits are supplied to the receiver frequency conversion circuits to retain the phase reference for each PRT.

c. **High voltage pulse generation circuits.** These are conventional HV pulse circuits (B4, fig 2) which use DC resonant charging and a "holdoff" diode to charge a pulse forming network (PFN) to twice the applied voltage. The big difference in the high voltage (HV) pulse generation in this transmitter from other radar transmitters is that four pulse forming networks are used. They charge in parallel and discharge in series-parallel combination to develop a wider pulse than would be possible with only one PFN. Mod trigger causes a pair of thyratron tubes to ionize, discharging the PFN's through a 7 to 1 step-up high voltage pulse transformer. This negative high voltage pulse is applied to the cathode of the klystron power amplifier while the final RF drive signal is applied to the input cavity of the klystron. Reverse-voltage and trigger-killer circuits are provided to open the high voltage interlocks if excessive mismatch occurs between the PFN's and the high voltage pulse transformer.

d. **Klystron power amplifier.** The klystron power amplifier converts the HV pulse and final RF drive into a burst of RF energy at the frequency of the final drive and for the duration of the HV pulse. This amplifier is broadbanded to accommodate all the L band frequencies available from the RF generation circuits. The seven resonant cavities in this klystron are broadbanded by RF loading and stagger tuning which also prevents the cavities breaking into oscillations at some undesired frequency. A beam of high speed electrons (fig 6) is accelerated toward the collector by

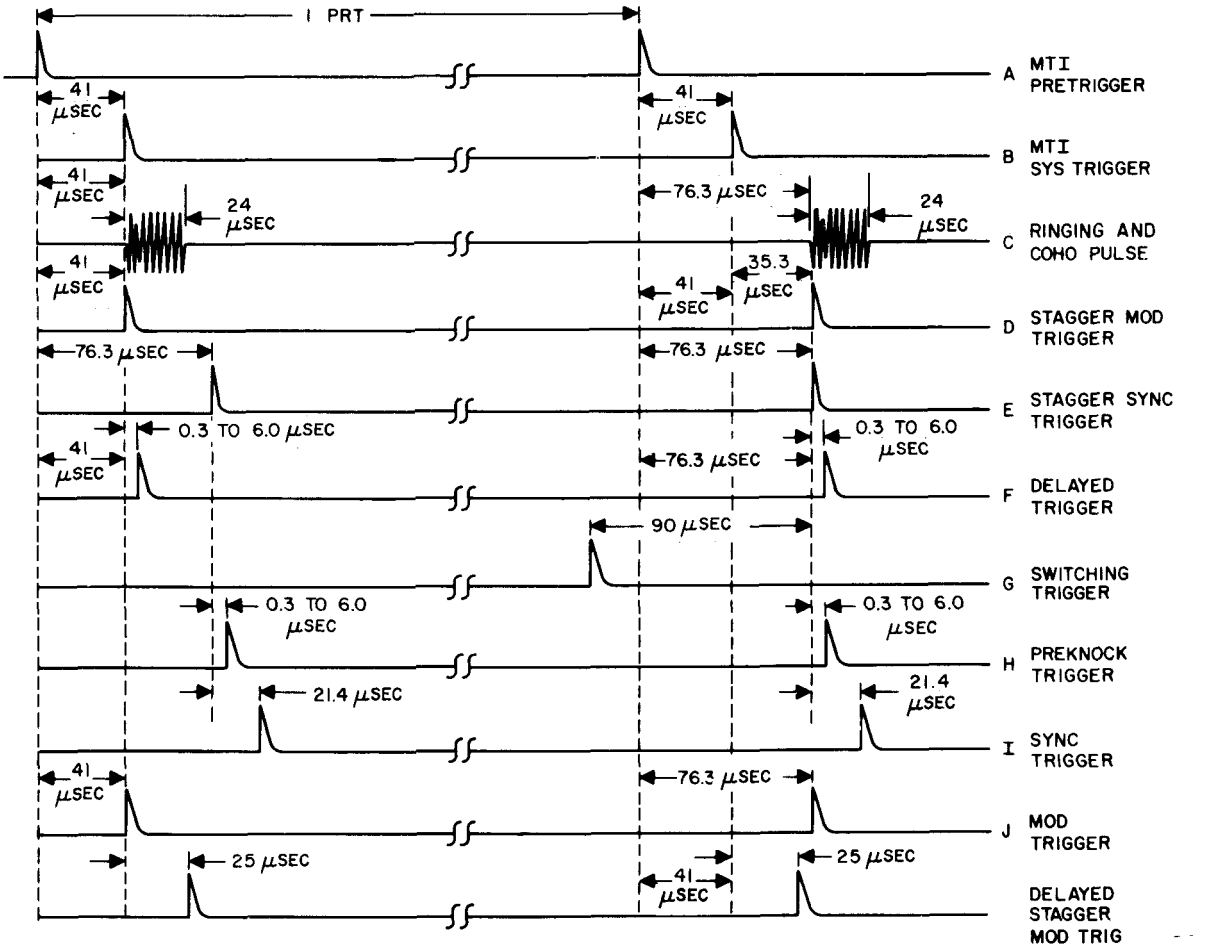


Figure 5. Synchronizer system - stagger operation - timing diagram.

the application of the HV pulse. This electron stream is centered in the drift tube by a magnetic field developed when a direct current is applied thru the field coils. The final RF drive, applied to the input cavity, establishes a field which alternately aids and opposes acceleration of electrons in the stream. This action causes a bunching effect on electrons in the drift tube. As the first electron bunch arrives at the output cavity, an oscillation is induced in the cavity. A second bunch of electrons arrive at this cavity just as the oscillating field is in a direction to oppose motion of the electrons. As the second bunch of electrons slow down due to this opposition, they give up energy to the output cavity. This energy is coupled from the output cavity through the waveguide components to the antenna while the slowed electrons continue to the collector. The transmitter RF may be switched into a dummy load. The dummy load and the klystron power amplifier are cooled by circulating a cooling solution through cooling jackets. The klystron is housed in a lead shield to reduce X-ray radiation hazard.

e. Waveguide components.

(1) General. When the transmitter RF energy leaves the klystron, it encounters three directional couplers--a harmonic filter, a duplexer, and a waveguide switch in the waveguide--before being sent to the CSC2 or FAN antenna.

(2) Directional couplers. The directional couplers are bidirectional devices that pass transmitter RF to the RF harmonic filter unattenuated while attenuating forward and reverse power signals that are applied to a voltage standing wave ratio (VSWR) monitor assembly and RF monitoring circuits. When reverse power is excessive, due to impedance mismatch or waveguide arcing, the VSWR signal operates a trip-out circuit in the VSWR monitor assembly that disables the transmitter RF by removing final RF drive from the klystron power amplifier. A transmitter RF signal and forward and reverse power signals are sent to transmitter

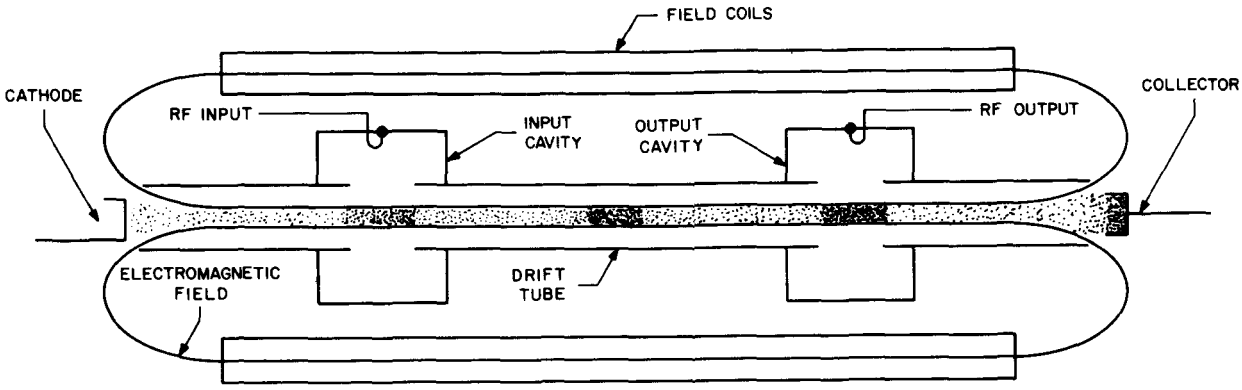


Figure 6. Klystron power amplifier - simplified diagram.

system RF signal monitoring circuits for monitoring transmitter performance.

(3) Harmonic filter. This filter consists of four muffler filters, one designed to attenuate the second harmonic, one the third harmonic, and the other two to attenuate the higher harmonics. Each filter consists of a series of slots in the waveguide that are cut to pass harmonics of the transmitted frequency into a resistive load where this energy is dissipated.

(4) Waveguide switch. A motor driven shutter in the waveguide directs transmitted energy into a dummy load or a rotary joint assembly to the antenna.

(5) Duplexer. The duplexer (fig 7) functions as a transmit-receive (TR) and an antitransmit-receive (ATR) device. Energy from the transmitter is horizontally polarized (horizontal "E" field) in the rectangular waveguide. The transition section converts the RF energy to circular propagation without changing

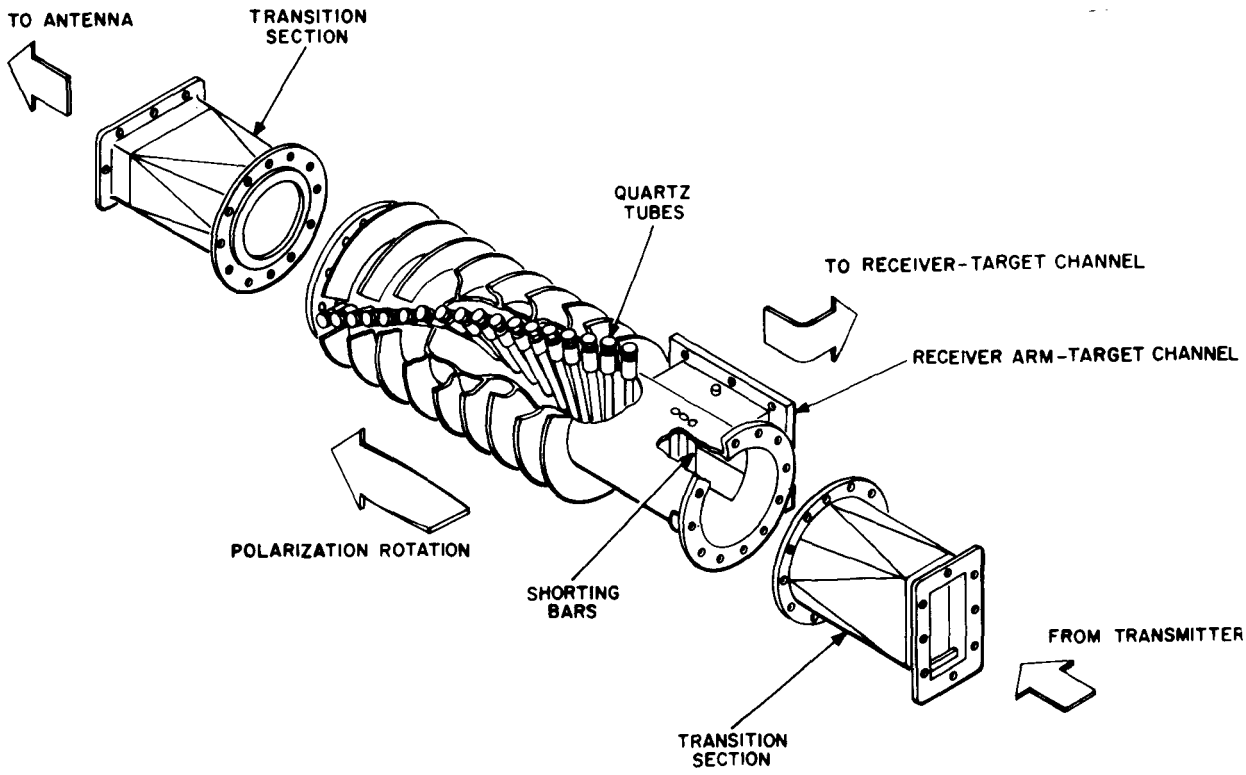


Figure 7. Duplexer assembly - cutaway view.

polarization. As the RF wavefront passes through the circular section of the duplexer, it strikes the shorting bars with the "E" field perpendicular to the bars. The receiver arm is constructed to receive a vertically polarized wave; therefore, only a small amount of transmitted energy, which is held horizontally polarized by the shorting bars, will enter the receiver. After passing the shorting bars, the transmitted wavefront strikes the first of 18 quartz tubes which form a 90 degree helix. The tubes are filled with argon gas which is ionized by the high power signal and appear as a series of shorting bars. The spiral configuration of these shorting bars causes the polarization of the RF energy to be rotated 90 degrees. The vertically polarized wave is now fed through the transition section into a vertically polarized rectangular waveguide to the antenna. Received energy from the antenna passes through the transition section and, due to its low power level, does not ionize the quartz tubes. This allows the energy to remain vertically polarized. When the received energy strikes the shorting bars, with the "E" field parallel to the bars, it is shorted in the transmitter arm and reflected into the vertically polarized receiver arm.

4. **ANTENNA SYSTEM.** The antenna system for the HIPAR consists of one active (main) antenna and three passive (omni and auxiliary) antennas which are illustrated in figure 8.

a. **Main antenna.** The main antenna, consisting of a rotary joint, feedhorn, and antenna reflector, serves both as a transmitting and receiving antenna. The antenna focuses the transmitted RF energy into a narrow beam to provide accurate azimuth scanning. The antenna may be a CSC^2 configuration for use against aircraft type targets or a FAN configuration for use against ASM or TBM type targets. The FAN configuration is sometimes called the ATBM antenna. Resolver signals from the main antenna drive system are supplied to the presentation system to synchronize the sweep voltages. Antenna rotation is 6.67 or 10 RPM.

b. **Omni antenna.** The omni antenna is a passive antenna that is used in conjunction with the main antenna to provide signals to the receiver strobe channel. Signals from the omni antenna are also used in the receiver multiple side lobe cancellation circuits (MSLC). The omni antenna is mounted above the top center of the main antenna (fig 8).

c. **Auxiliary antennas.** The two auxiliary antennas are passive CSC^2 antennas. They are mounted atop the main antenna and rotate with the main antenna. The auxiliary antennas respond to signals that are received in the main antenna side lobes. The signals from these antennas are used for comparison with the main antenna signals in the MSLC.

5. **RECEIVING SYSTEM.**

a. **General.** The receiver is supplied RF energy from the four antennas thru four noise couplers in the waveguide assembly. The main antenna signal is reflected into the feedhorn, thru the waveguide, and duplexer to the main receiver. The remaining three antennas are connected to the receiver thru heliex conductors. The noise couplers are used for the injection of noise into a selected receiver channel during a receiver noise figure test. To protect the receiver from damage during transmit the main receiver input is provided with a TR tube, the omni and auxiliary receivers are provided with RF limiters.

b. **Frequency conversion circuits.** The frequency conversion circuits (C3, fig 2) convert all received RF (L-band) signals into 30-MHz IF signals. These circuits use dual conversion and parametric amplification to derive the IF signals. Dual conversion provides good image frequency rejection and parametric amplification provides high gain for received RF signals without appreciable noise insertion. Two parametric assemblies are used with two amplifiers in each assembly. One assembly is used for the main and omni antenna signals while the other is used for the auxiliary antenna signals. Each parametric amplifier assembly uses a common CW pump (X-band) signal and common CW STALO RF signal, from the RF generation circuits (C3, fig 2), to convert receiver RF signals to 142-MHz IF. Figure 9 illustrates the principle upon which the parametric amplifier operates. The varactor mount (amplifier-converter shown in figure 9) converts the main-received RF signal into an amplified X-band output signal. The varactor diode is a solid state device whose capacitance (cv) varies nonlinearly as a function of the applied voltage. As the pump signal is applied, it changes the width of the depletion region thereby changing the capacitance of the varactor diode. Since the amplitude of the pump signal is many times greater than the receiver RF signal, it can be assumed that the pump signal supplies most of the energy stored in the varactor capacitance. The pump signal being CW is always present but the received signal is present only when an echo or jamming signals are being received. Therefore, the idler circuit, which is tuned to the difference between the received RF and the X-band pump signal, produces an output only when target echos or jamming is being received. On one alternation of the pump signal, the width of the depletion region is reduced (action similar to pushing a capacitor's plates together) and the

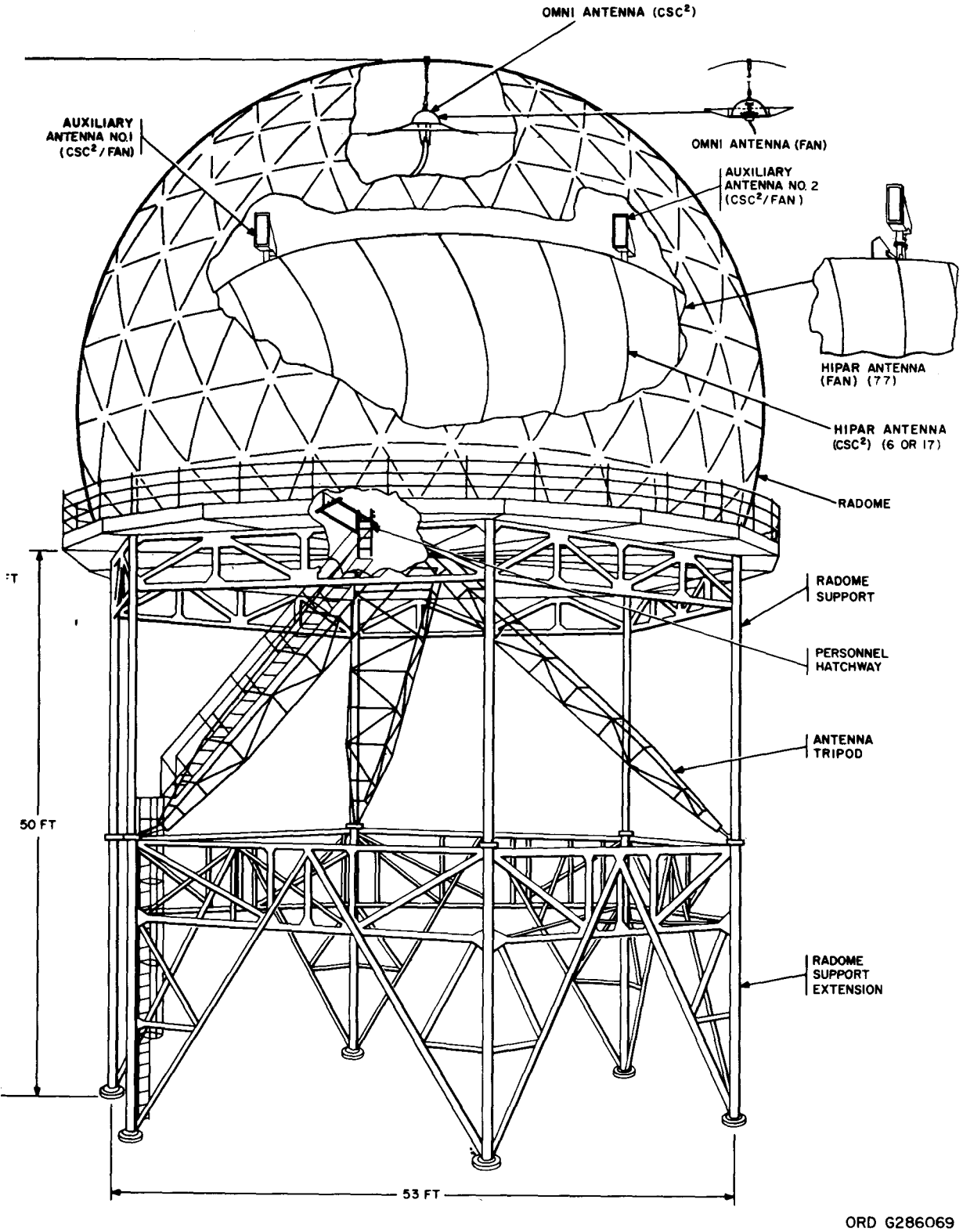


Figure 8. Radar antenna support set and radome - location diagram.

increased capacitance is charged by the received RF signal. When the pump signal changes polarity, the depletion region widens (action similar to pulling a capacitor's plates apart) and the capacitance is lowered quickly. Since Q, in the formula Q = CE, cannot change, E (signal voltage) must increase, producing the desired amplification of the received RF signal. The output from the idler circuit is heterodyned in a balance mixer with another X-band frequency which was produced by mixing the pump with the STALO RF. The balance mixer produces a 142-MHz IF which is mixed, in an amplifier-converter, with the 112-MHz CW from the RF generation circuits. The final conversion produces a 30-MHz IF. The main and omni IF's are applied to the receiver strobe channel (D6, fig 2) while the main, omni and two auxiliary signals are applied to the multiple side lobe cancellation circuits (MSLC) which are included in the RF conversion circuits.

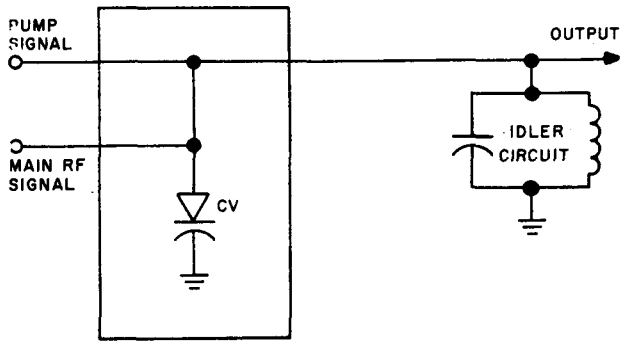


Figure 9. Varactor mount - simplified diagram.

c. **AJAC receiver.** The automatic jamming avoidance circuits (C4, fig 2) have a separate receiver and RF conversion circuits. The input to the AJAC receiver is from the main antenna but is prior to the main parametric amplifier. Therefore, the AJAC receiver is capable of responding to all channels that the radar is transmitting on independently of the transmitter tuning. The AJAC receiver supplies video information to the AJAC programmer.

d. **Strobe channel.**

(1) The primary purpose of the strobe channel circuits is to produce a jam strobe on the presentation system at the azimuth of the jamming source. This jam strobe is produced only when the CSC2 or FAN main antenna is alined with a jammer.

(2) A representation of the lobe structure for a typical acquisition antenna is shown in A, figure 10. In addition to the main lobe, the acquisition antenna has many side lobes, each capable of receiving energy. Without special circuits, energy received from a jammer by side lobes would produce many strobe lines on PPI displays, preventing accurate azimuth indications of a jammer. Generation of jam strobes, due to side lobe reception, is prevented by circuits in the strobe channel which compare power received from the main and omni-antennas.

(3) The omni-antenna pattern (B, fig 10) is superimposed on the main antenna pattern. The omni-antenna provides equal gain in all directions, but some side lobes of the main antenna have a higher gain than those of the omni-antenna (B, fig 10). To prevent these higher gain side lobes from producing strobes, the main received energy is attenuated (offset) so that energy received by the strongest side lobe is less than energy received by the omni-antenna (C, fig 10).

(4) The strobe circuits (fig 2) heterodyne energy received from the main antenna to a 21-MHz IF and energy received from the omni-antenna to a 19-MHz IF. These two IF frequencies are applied to a discriminator that produces an output whose polarity is determined by the frequency of the strongest input and whose amplitude is determined by the strength of the strongest input. If 21-MHz is stronger in amplitude, the discriminator output will be positive; however, if 19-MHz is stronger, the output will be negative. Further, if the main lobe is pointed away from a jamming source, the 19-MHz IF will be stronger. Only a positive output from the discriminator can be processed into MJS video, therefore indicating azimuth of a jammer. The MJS video is destaggered by gate triggers No 1 and No 2 during stagger operation.

(5) During normal operation, MJS video is mixed with MTI and integrator video in the video mixer which is part of the target channel. During JS only, MTI and integrator video are removed from the video mixer and only MJS video appears as system video output. During basic receiver operation, the MJS video is removed from the video mixer.

e. **Multiple side lobe cancellation circuits.**

(1) The MSLC circuits use the main, omni, auxiliary 1, and auxiliary 2 30-MHz IF signals from the frequency conversion circuits to provide jamming protection for the 30-MHz main IF signal. These MSLC circuits are part of the RF conversion block at D3, figure 2.

(2) Three identical cross-correlation cancellation loops are used to increase target signal detection in the main receiver channel by cancelling

noise and interference (jamming) which reach the main receiver channel through the side lobes of the main antenna. Cancellation in each loop is the result of narrow band filtering and phase shifting of the omni and auxiliary signals then comparing the resultant signal with the main received signal. The resultant signal, which is the main received signal, is applied to the target channel and the MTI signal processing circuits as a 30-MHz IF (C8 and C9, figure 2).

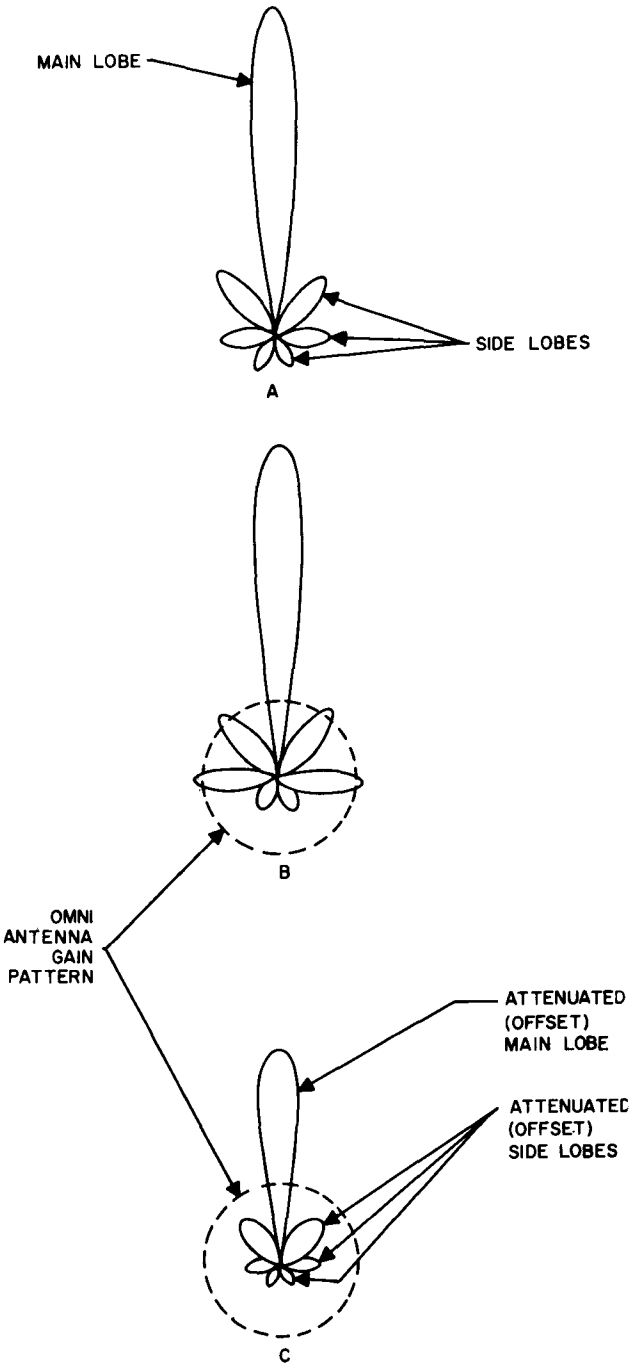


Figure 10. Main lobe indicator - antenna pattern.

f. Target channel.

(1) The target channel (C8, fig 2) of the receiver processes the main 30-MHz IF signal into a video signal which is applied as the system video to the monitor PPI circuits (C12, fig 2) and the presentation system (A13, fig 2).

(2) The target channel is a complete processing channel and is one of three processing circuits contained in the AJI HIPAR system. The strobe and MTI signal processing circuits are the remaining two signal paths.

(3) During normal operation (AJD mode), the target channel circuits route the 30-MHz main IF signal to the MTI signal processing circuits and receive the MTI processed main IF signal for detection into a video signal. The target channel produced video signal is reapplied to the MTI signal processing circuits for video integration by the integrator circuits. The MTI and integrator processed video is returned to the target circuits and is mixed in a video mixer with the jam strobe video from the strobe channel circuits to provide the system video signal.

(4) During the AJAC pulse-to-pulse or standby receiver modes of operation, the MTI signal processing circuits are bypassed and the 30-MHz main IF signal is processed through Dicke-fix, FAGC, and STC anti-jamming circuits in the target channel to produce the system video output.

(5) When the basic receiver mode of operation is selected, the MTI system, strobe channel circuits, and anti-jamming circuits in the target channel are bypassed, and a normal video signal is processed by the target channel circuits.

6. AJAC CIRCUITS.

a. The automatic jamming avoidance circuits (AJAC) provide a means of avoiding active ECM. The circuits consist of an independent secondary receiver coupled to a small special purpose computer. All actions for the avoidance of ECM are performed by the computer (AJAC Programmer).

b. For detailed information on the operation of these circuits refer to TM 9-1430-254-12/8 and TB 9-1430-254-12/3.

7. MOVING TARGET INDICATOR SYSTEM.

a. Destagger circuits (B8, fig 2) receive the

30-MHz from the Dicke-Fix circuits in the MTI signal processing circuits. During normal operation (stagger on), the destagger circuits return the staggered IF to a uniform time base. The destaggering process is required to obtain proper phase relationships (coherence) for cancellation of stationary targets and clutter. Destaggering is accomplished by applying the stagger-delay interval (para 2d(1)(2)) to the IF returns that are not delayed (alternate PRT's) prior to transmission. Synchronization is assured by using the stagger triggers generated for the stagger firing of the transmitter (fig 5).

b. MTI signal processing circuits.

(1) Purpose. The MTI signal processing circuits (C9, fig 2) compare target-return signals to distinguish fast-moving target returns from clutter. Clutter signals are cancelled or greatly attenuated, while fast-moving target returns are processed for display in the presentation system. Three processing techniques are used to distinguish moving-target returns from fixed-target (clutter) returns. These are coherent signal processing, ACET signal processing, and video integrator signal processing. These techniques are in series and can be inserted or bypassed on an individual basis.

(2) Coherent signal processing circuits of the MTI receive the 30-MHz IF from the MTI Dicke-Fix circuits. The Dicke-Fix circuits reduce the effect of certain jamming signals thru the use of wide band amplification, hard limiting and narrow band filtering. Coherent signal processing compares phase differences between successive target return signals. This comparison consists of delaying the first target-return signal one PRT plus 180 degrees and then combining the signal with the next target-return signal. Return signals reflected from fixed targets have the same phase for two successive returns and, by delaying the first target-return signal, the two signals are 180 degrees out of phase (a, fig 11) causing them to cancel. The reflected returns from a moving target are out-of-phase for successive returns, delaying the first return pulse one PRT plus 180 degrees does not cause the two signals to be exactly 180 degrees out-of-phase. Consequently, when combined, complete cancellation does not occur and the resultant residue signal represents the moving target. To insure complete cancellation, of fixed targets, two cancellation loops are used.

(3) Automatic cancellation of extended target circuits (ACET) have a purpose similar to that of the MTI coherent cancellation circuits. The ACET circuits, through the use of a cross- correlation cancellation loop, cancel target returns with an extended time base over normal target returns. A simplified block diagram of the ACET circuit is shown in figure 12. In the ACET circuit, each return signal is delayed one PRT by a delay line and then cross correlated with the next undelayed return from the same target. If correlation occurs over a period of time longer than the cross correlation loop (9 to 12 microseconds), the target is considered clutter. When this situation exists, the amplitude and phase of the delayed returns are adjusted so that they cancel all but the first 9 to 12 microseconds of the undelayed signal. After processing in the ACET circuits the signal is then applied thru the fast automatic gain control circuits (FAGC) to canceller loop two. The

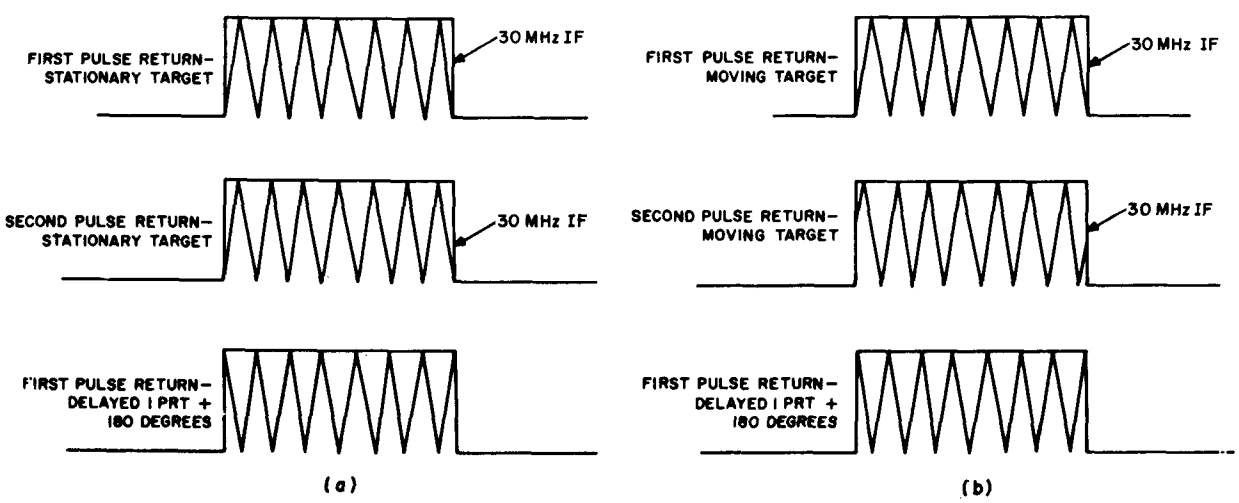


Figure 11. Phase relationship of successive fixed and moving target returns.

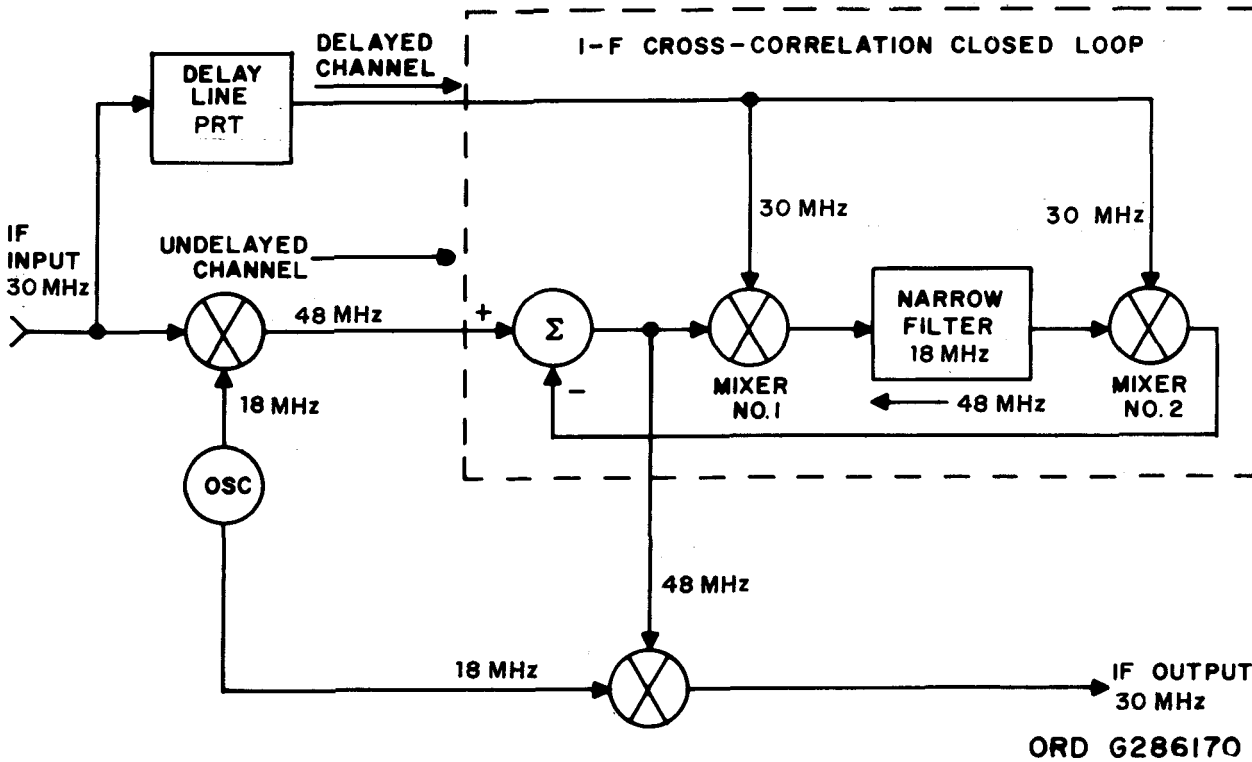


Figure 12. ACET circuit - simplified block diagram.

FAGC circuits are used, the same as in other radars, to overcome the effect of CW and slow sweep type of ECM. After the 30-MHz IF signal has been processed in the MTI signal circuits it is returned to the receiver cabinet where it is amplified thru additional FAGC circuits and then processed in the receiver video detector. Video signals are then sent to the MTI video integrator circuits.

(4) MTI video integrator circuits, as part of the signal processing circuits, use a process of signal addition that enhances the amplitude of nonlimited signals and discriminates against nonsynchronous signals (noise). Integration is performed by modulating a 20-MHz carrier with the signal video then delaying the signal by one PRT. The delayed signal is then applied to the nondelayed signal in such a way that the synchronous video is added and the nonsynchronous (noise) is not. Video is then detected from the 20-MHz signal.

(5) MTI gating circuits control the action of the MTI signal processing circuits on a time basis. The gating circuits employ three switching chassis activated by MTI-pretrigger and MTI negative range trigger. The canceller circuits (para 7b(2)) are gated on with the application of pre-trigger and bypassed starting at the negative range trigger time. Negative range trigger is variable in time from 50 to 1700 microseconds after MTI system trigger. All signals, after range trigger, bypass the coherent cancellation loops and are processed in the video integrator circuits. The ACET and FAGC circuits are in use for the full PRT. As a result of the MTI gating circuits, the video applied to the presentation system will be as shown in figure 13.

(6) MTI performance monitoring circuits (B10, fig 2) provide performance-level indications of two major system signal processing characteristics. The minimum discernible signal (MDS) monitor section checks the signals which are processed through the chain consisting of the RF conversion circuits and either the target channel or the MTI signal processing circuits for any transmitted frequency. The results of the check is read as a -DBM on a meter mounted in the MTI cabinet. The cancellation ratio (CR) monitor section checks either the MTI canceller No 1 performance including the transmitter pulse-to-pulse phase stability or the ACET canceller performance. The MTI-CR and ACET-CR performance levels are indicated in the form of a relative

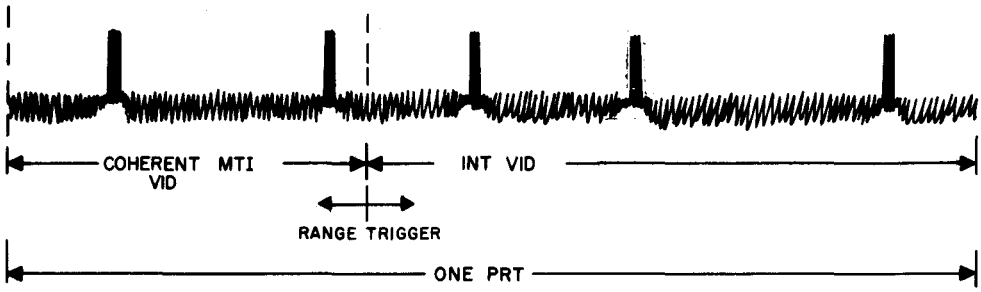


Figure 13. Typical AJI HIPAR display.

figure of merit. Only MTI canceller No 1 is checked. Provisions are also provided in the performance monitoring circuits to check the operation of the AJAC circuits.

8. **PRESENTATION SYSTEM.** You should recall from the LOPAR lesson that two different presentation systems may be found in the Nike System. One being known as the improved Nike Hercules and the other as the ATBM presentation system. The block diagram shown under coordinates 13 and 14 of figure 2 is a simplified illustration of the ATBM presentation system. Since the same information is displayed on both, a repeat of the BCC presentation will not be given in this lesson. However, video monitor circuits located in the HIPAR building and illustrated at (D12) figure 2 will be discussed.

a. **General.** The video monitoring circuits that are used only for test purposes consist of the video and sweep circuits as shown in figure 14. The video circuits permit selection of either system, strobe, signal, normal or gated MTI, and integrated video for monitoring and display. These circuits also develop rangemarks that intensity-modulate the radial sweep on the HIPAR monitor PPI. The rangemarks, which appear as concentric rings on the rotating sweep, provide a means of checking target range. The sweep circuits produce the radial sweep on the HIPAR monitor PPI.

b. **Sweep circuits.** The radial sweep is synchronized in time with HIPAR operation and in azimuth with the CSC^2 or FAN acquisition antenna rotation. These circuits consist of a gate intensifier, sweep generator, focus assembly, focus coil L2, deflection coil L1, azimuth-position motor B2, servoamplifier, and control synchro B1. The sweep circuits produce a timing gate, a sweep deflection voltage, a focus current, and a blanking pulse.

(1) A sync trigger from trigger synchronizing circuits is applied to the gate intensifier. This trigger synchronizes the operation of the sweep circuits with that of the HIPAR. The negative timing-gate output of the gate intensifier is applied to the sweep generator is the sweep circuits and to the rangemark generator and CRT indicator V1 in the video circuits. The sweep generator produces a sweep-deflection voltage that is applied to deflection coil L1 and a blanking pulse that is applied to the gate intensifier to terminate the timing gate. The sweep generator also receives rangemarks from the rangemark generators that are used to produce the blanking pulse when the sweep reaches a predetermined range. The duration of the sweep-deflection voltage, which is equal to the duration of the timing gate from the gate intensifier, determines the electrical length (sweep time) of radial sweep. The amplitude of the sweep-deflection voltage determines the physical length of the radial sweep.

(2) A resolver in the antenna azimuth drive circuits supplies azimuth position through a control transformer and servoamplifier to an azimuth position motor at the CRT indicator. The azimuth position motor turns the CRT deflection coil which causes the radial sweep to rotate in sync with the CSC^2 or FAN antenna.

(3) Focus coil L2 receives focus current from the focus assembly. By regulating the current flow through L2, the focus assembly controls the focus of video and sweep on CRT indicator V1.

c. **Video circuits.** The video circuits (fig 14) provides the means of selecting the type of video signal to be displayed and produce the rangemarks. These circuits also amplify and display the rangemarks and selected video. The video circuits consist of the rangemark generator, the PPI video amplifier, CRT indicator V1, and PPI video SELECTOR switch S4.

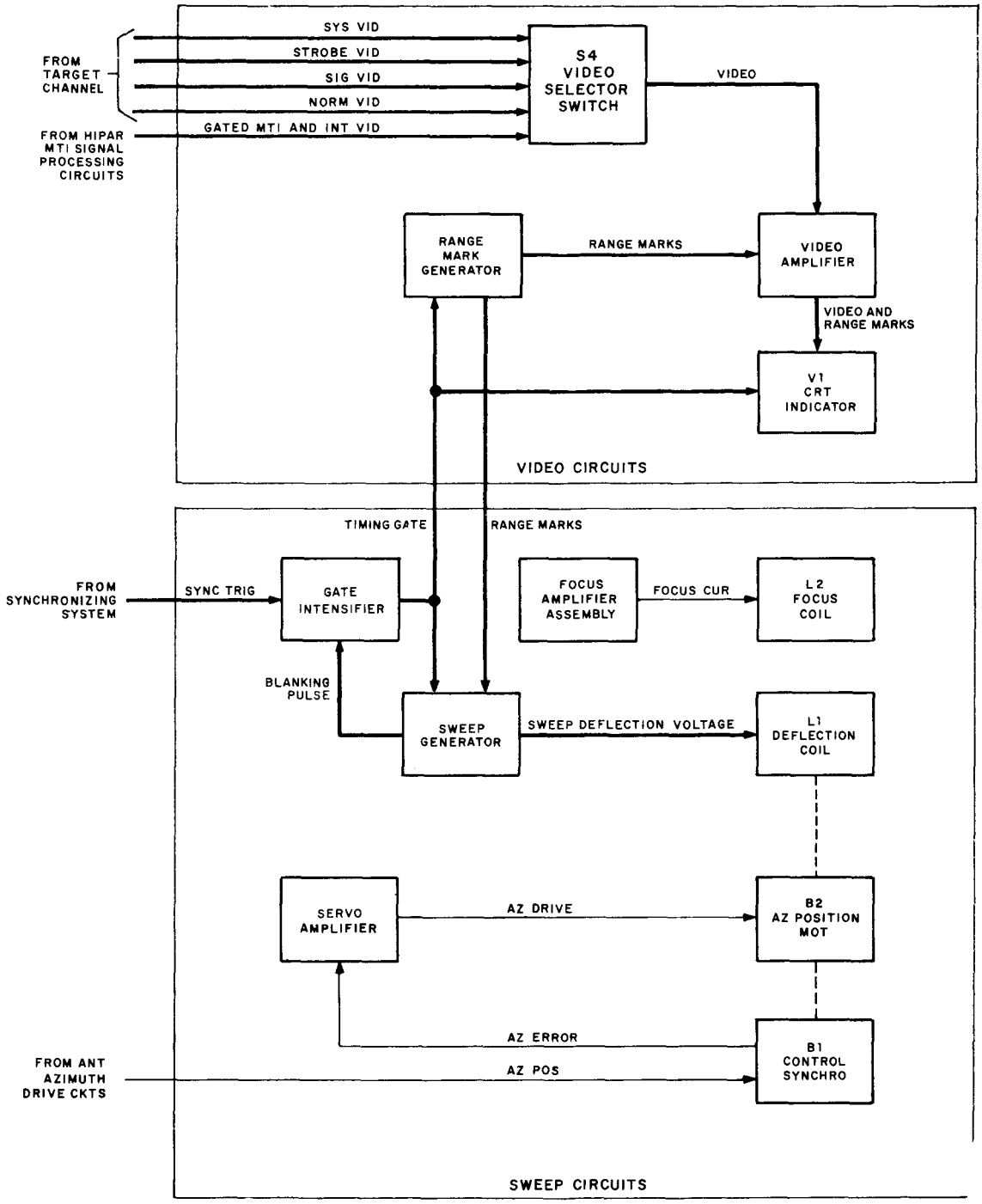


Figure 14. Video monitor circuits - block diagram.

(1) PPI VIDEO SELECTOR switch S4 is used to select gated MTI and integrator, normal, signal, strobe, or system video. The selected video is applied through S4 to the PPI video amplifier.

(2) The rangemark generator is switched on by the timing gate from the gate intensifier, producing rangemarks at 50,000-yard intervals. The interval between rangemarks is determined by the

frequency of an oscillator in the rangemark generator; the number of rangemarks produced is determined by the duration of the timing gate. The rangemarks are applied to the PPI video amplifier, where they are mixed with the selected video, and to the sweep generator in the sweep circuits to insure termination of the timing gate at the proper time.

(3) The PPI video amplifier combines the selected video with the rangemarks. The combined video and rangemarks are amplified by the PPI video amplifier and applied to CRT indicator where they intensity-modulate the radial sweep. The timing gate applied to the CRT unblanks it during sweep time and allows video to be presented.

MMS SUBCOURSE NUMBER 150, NIKE RADARS AND COMPUTER

EXERCISES FOR LESSON 3

1. By which method is the HIPAR monitor PPI sweep rotated?

   A. 90 degrees out of phase deflection voltages applied to L1
   B. 90 degrees out of phase deflection voltages applied to L2
   C. Rotation of L1
   D. Rotation of L2

2. Which pulse or pulses is/are applied to the HIPAR trigger sync circuits during normal operation, with stagger on?

   A. Stagger mod and stagger sync triggers
   B. Preknock
   C. Stagger sync trigger
   D. System trigger

3. What is the purpose of the stagger circuits?

   A. Eliminate clutter
   B. Overcome blind speeds
   C. Improve signal to noise ratio
   D. Synchronize the AJAC

4. While in the operate condition, the HIPAR transmitter frequency may be changed from which location?

   A. Trailer mounted director station
   B. HIPAR building
   C. Radar control trailer
   D. Transmitter control indicator

5. Which system is shared by HIPAR and LOPAR?

   A. Synchronizing
   B. Antenna
   C. MTI
   D. Presentation

6. Which circuits in the AJI HIPAR reduce the threat of ECM entering the sidelobes of the main antenna?

   A. AJAC
   B. ACET
   C. MSLC
   D. SILOFAB

7. Rapid changes in transmitter RF are possible by changing which frequency?

   A. Pulse repetition
   B. Stable local oscillator
   C. Switching trigger
   D. COHO

8. If the HIPAR radar is selected, what triggers the acquisition track synchronizer in the target tracking radar?

   A. Stagger sync trigger
   B. Stagger mod trigger
   C. System trigger
   D. Preknock trigger

9. What determines the number of rangemarks on the video monitor CRT?

   A. Duration of the timing gate
   B. The amplitude of the sweep voltage
   C. The type video selected
   D. Time between sync pulses

10. What is the delay interval, in microseconds, applied to alternate high voltage pulses during normal operation, with stagger on?

A. 20
B. 21.4
C. 35.3
D. 41.3

11. Which pulse times the trigger sync circuits during the normal mode, with stagger off?

A. Sync
B. MTI system
C. Preknock
D. MTI pretrigger

12. During which condition is the HIPAR trigger synchronizer free running?

A. Stagger on
B. Stagger off
C. Standby
D. MTI on

13. What is the purpose of the delay trigger output of the HIPAR synchronizing system?

A. To center (final) RF drive under the high voltage pulse
B. Compensate for inherent delay in the video circuits during normal operation
C. Allow changing transmitter frequency during dead time
D. Determine transmitter pulse width

14. During what portion of a PRT are the ACET circuits in use?

A. Full PRT
B. 9 to 12 microseconds
C. 35.3 microseconds
D. 70 microseconds

15. When performing the MDS check, how are the results expressed?

A. -microvolts
B. -DBM
C. Micromicro volts
D. DBM

16. What determines the output polarity from the discriminator in the strobe channel of the HIPAR receiver?

A. Frequency of the strongest input
B. Polarity of the strongest input
C. Main antenna pattern
D. Auxiliary antenna pattern

17. Which trigger discharges the PFN's in the high voltage pulse network?

A. Sync
B. Delay
C. Mod
D. Preknock

18. What part of the HIPAR provides the input to the AJAC receiver?

A. Omni antenna
B. Main antenna
C. Parametric amplifier
D. IF distribution circuits

19. What circuits check the cancellation ratio of MTI canceller No 1?

A. AJAC
B. ACET
C. Performance monitor
D. Presentation

20. What is the maximum time that MTI video may be displayed on the presentation system?

A. 50 microseconds
B. 70 microseconds
C. 1,500 microseconds
D. 1,700 microseconds

21. Received energy passing through the duplexer is

A. horizontally polarized.
B. rotated 90 degrees.
C. vertically polarized.
D. shorted by the quartz tubes.

22. How is the perfect synchronization of staggering and destaggering accomplished?

A. By applying the stagger delay interval to all return pulses
B. By time sharing a common time delay circuit
C. By applying the stagger delay interval to received pulses produced by delayed transmitter pulses
D. By applying the stagger delay interval to received pulses produced by nondelayed transmitted pulses

23. Which permits time sharing of the 1 PRT delay line in the MTI trigger generation circuits with the MTI system?

A. Final RF drive
B. COHO pulse
C. Delay trigger
D. Guard gate

24. What frequencies are heterodyned in the frequency conversion circuits to produce the 30 MHz IF for the receiver?

A. 142 and 112 MHz
B. 142 and X-band pump
C. 112 and STALO
D. 112 and COHO

25. Which pulse phase locks the transmitter and MTI system with stagger on?

A. STALO
B. High voltage
C. COHO
D. 142 MHz